

## Product Specification

# SPECIFICATION FOR APPROVAL

(●) Preliminary Specification

( ) Final Specification

Title	86.0" QWUXGA TFT LCD
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BUYER	CM-CH
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LC860EQY
SUFFIX	FJA6 (RoHS Verified)

APPROVED BY	SIGNATURE	DATE
/		
/		
/		

Please return 1 copy for your confirmation with your signature and comments.

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**LG Display Co., Ltd.**



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## Product Specification

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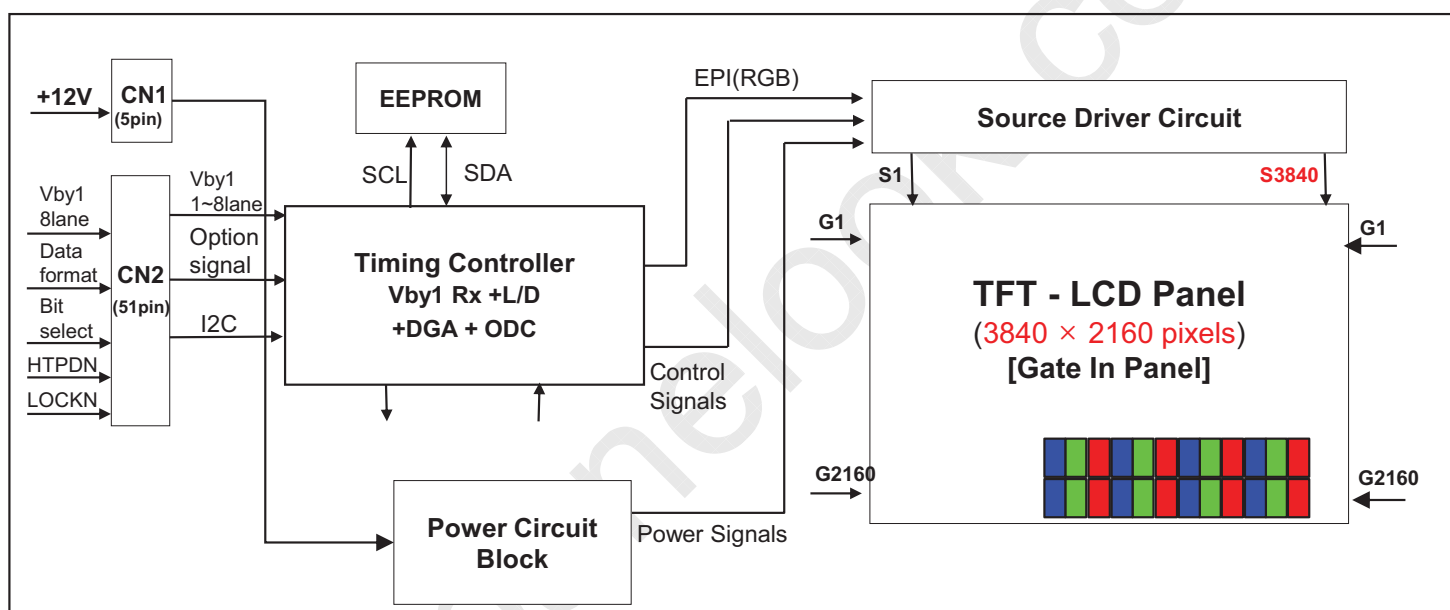
## Product Specification

## 1. General Description

The LC860EQY is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 85.60 inch diagonally measured active display area with QWUXGA resolution (2160 vertical by 3840 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 10bit gray scale signal for each dot. Therefore, it can present a palette of more than 1.07 billion colors.

It has been designed to apply the 10-bit 8 Lane VbyOne interface.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



## General Features

Active Screen Size	85.60 inches(2174.27 mm) diagonal
Outline Dimension	(1913.0(H) x 1084.0 (V) x 1.3 (D) mm(Typ.)
Pixel Pitch	0.4935 mm x 0.4935 mm
Pixel Format	3840 horiz. by 2160 vert. Pixels, RGB stripe arrangement
Power consumption	Total 690.W(Typ)
Lunminance,White	2000cd/ ( Center 1point,typ)
Transmittance(with POL)	5.42(TBD) %(Typ.)
Viewing Angle (CR>10)	Viewing angle free ( R/L 178 (Min.), U/D 178 (Min.))
Weight	5.9 Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment (Top)	Hard coating(2H), Anti-glare treatment of the front polarizer(Haze 28%(Typ.))
Possible Display Type	Landscape Only Enable

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## 2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	LCD Circuit	VLCD	-0.3	+14.0	VDC	1
T-Con Option Selection Voltage		VLOGIC	-0.3	+4.0	VDC	
Operating Temperature		TOP	0	+50	°C	2,3
Storage Temperature( <b>without packing</b> )		TST	-20	+60	°C	
Panel Front Temperature		TSUR	-	+68	°C	4
Operating Ambient Humidity		HOP	10	90	%RH	2,3
Storage Humidity		HST	5	90	%RH	

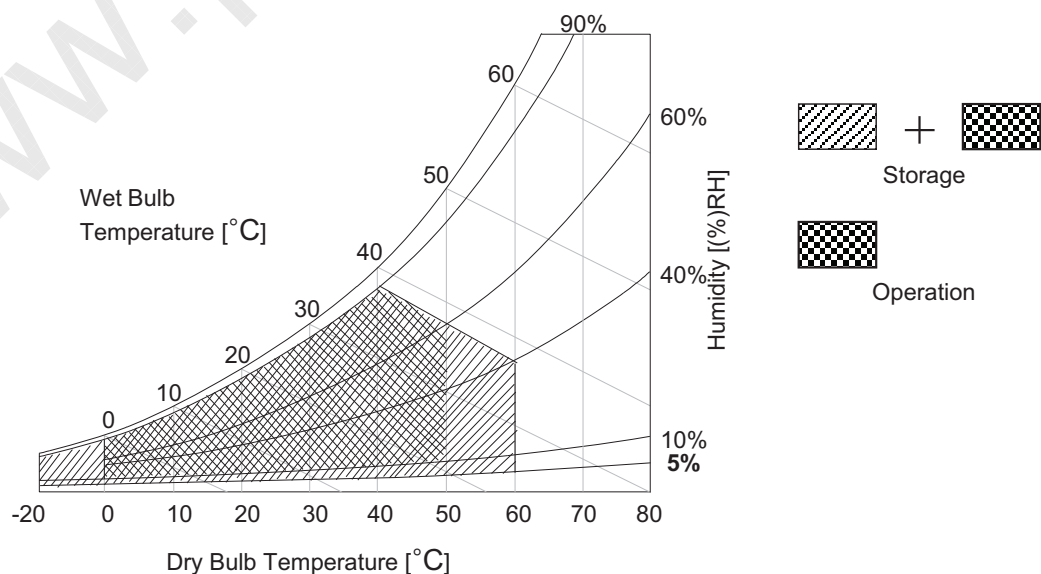
Note 1. Ambient temperature condition ( $T_a = 25 \pm 2^\circ\text{C}$ )

2. Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be Max  $39^\circ\text{C}$ , and no condensation of water.

3. Gravity mura can be guaranteed below  $40^\circ\text{C}$  condition.

4. The maximum operating temperatures is based on the test condition that the surface temperature of display area is less than or equal to  $68^\circ\text{C}$  with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over  $68^\circ\text{C}$ . The range of operating temperature may be degraded in case of improper thermal management in final product design.



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## Product Specification

## 3. Electrical Specifications

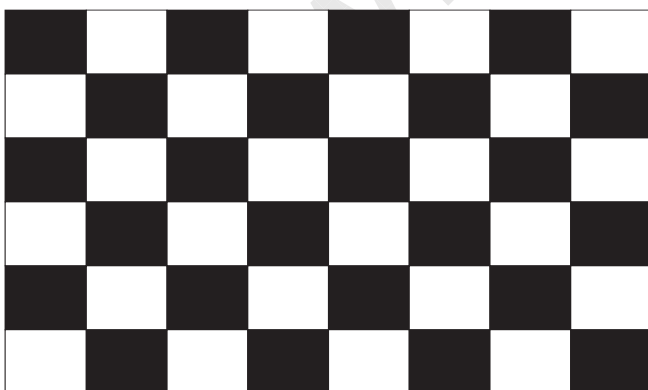
## 3-1. Electrical Characteristics

Table 2. ELECTRICAL CHARACTERISTICS

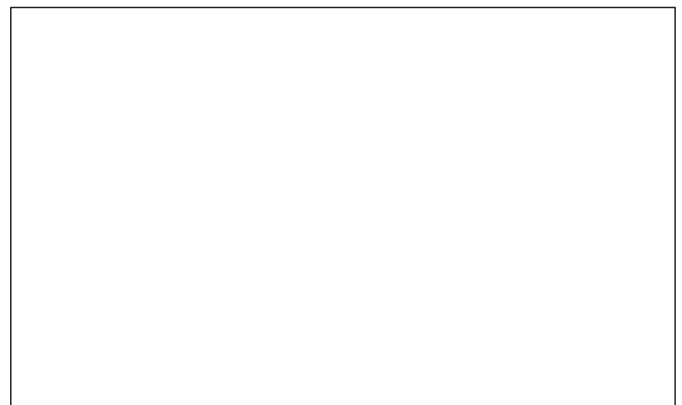
Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Circuit :							
Power Input Voltage		VLCD	10.8	12.0	13.2	Vdc	
Power Input Current		ILCD	-	1920 (TBD)	2496(TBD)	mA	1
			-	3110 (TBD)		mA	2
T-CON Option Selection Voltage	Input High Voltage	V <sub>IH</sub>	2.7	-	3.6	VDC	
	Input Low Voltage	V <sub>IL</sub>	0	-	0.7	VDC	
Power Consumption		PLCD	-	23.04 (TBD)	29.95 (TBD)	Watt	1
Rush current		IRUSH	-	-	12.0	A	3

- note 1. The specified current and power consumption are under the V<sub>LCD</sub>=12.0V, Ta=25 ± 2°C, f<sub>v</sub>=60Hz condition, and mosaic pattern(8 x 6) is displayed and f<sub>v</sub> is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The duration of rush current is about 2ms and rising time of power input is 0.5ms (min.).
4. Ripple voltage level is recommended under ±5% of typical voltage

White : 255 Gray  
Black : 0 Gray



Mosaic Pattern(8 x 6)



Max Current Pattern (Full White Pattern)

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### 3-2. Interface Connections

This LCD module employs three kinds of interface connection, 5-pin connector, 51pin connector are used for the module electronics

#### 3-2-1. LCD Module

- LCD Connector(CN1): 20037WR-H05 (manufactured by YEONHO)
- Mating Connector : SMH200-H05M (YEONHO) or compatible

**Table 3-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION**

Pin No	Symbol	Description	Note
1	GND	Ground	
2	GND	Ground	
3	VLCD	Power Supply +12.0V	
4	VLCD	Power Supply +12.0V	
5	VLCD	Power Supply +12.0V	

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- LCD Connector(CN2): FI-RXE51S-HF (manufactured by JAE)
- Mating Connector : FI-R51HL(JAE)

Table 3-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

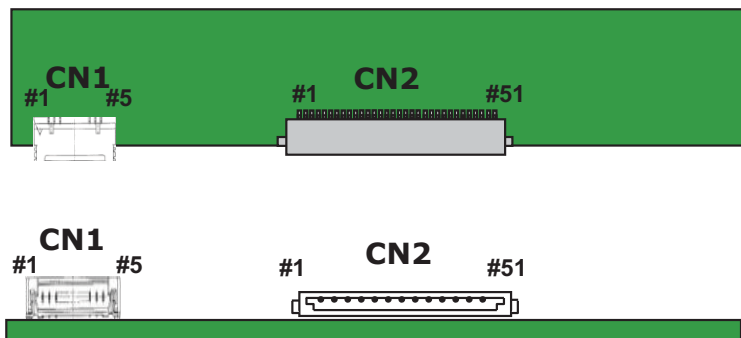
No	Symbol	Description	No	Symbol	Description
1	NC	No Connection(Notes 2)	27	GND	Ground
2	NC	No Connection(Notes 2)	28	Rx0n	V-by-One HS Data Lane 0
3	NC	No Connection(Notes 2)	29	Rx0p	V-by-One HS Data Lane 0
4	NC	No Connection(Notes 2)	30	GND	Ground
5	NC	No Connection(Notes 2)	31	Rx1n	V-by-One HS Data Lane 1
6	NC	No Connection(Notes 2)	32	Rx1p	V-by-One HS Data Lane 1
7	NC	No Connection(Notes 2)	33	GND	Ground
8	NC	No Connection(Notes 2)	34	Rx2n	V-by-One HS Data Lane 2
9	NC	No Connection	35	Rx2p	V-by-One HS Data Lane 2
10	GND	Ground	36	GND	Ground
11	GND	Ground	37	Rx3n	V-by-One HS Data Lane 3
12	GND	Ground	38	Rx3p	V-by-One HS Data Lane 3
13	GND	Ground	39	GND	Ground
14	NC	NO CONNECTION	40	Rx4n	V-by-One HS Data Lane 4
15	NC	NO CONNECTION	41	Rx4p	V-by-One HS Data Lane 4
16	NC	NO CONNECTION	42	GND	Ground
17	Input Mode	Vx1 Input Data Format 'L'=Non-Division , 'H'=2-Division	43	Rx5n	V-by-One HS Data Lane 5
18	SDA	SDA (For I2C)	44	Rx5p	V-by-One HS Data Lane 5
19	SCL	SCL (For I2C)	45	GND	Ground
20	NC	NO CONNECTION	46	Rx6n	V-by-One HS Data Lane 6
21	Bit_SEL	'H' = 10bit , 'L' = 8bit	47	Rx6p	V-by-One HS Data Lane 6
22	NC	NO CONNECTION	48	GND	Ground
23	RBF	'H' : AGP(Default), 'L' : NSB (No signal Black)	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect	-	-	-

- notes
1. All GND (ground) pins should be connected together to the LCD module's metal frame.
  2. #1~#8 NC (No connection) : These pins are used for back up power source, V<sub>LCD</sub> (power input) . These pins should be connected together.
  3. All Input levels of V-by-One signals are based on the V-by-One HS Standard Version 1.4.
  4. #16, #20, #22 NC (No Connection) : These pins are used only for LGD (Do not connect)
  5. About specific pin (#17, 21) , Please see the Appendix IV.
  6. Specific pin No. #23 is used for "No signal detection" of system signal interface.  
It should be GND or NC for NSB (No Signal Black) while the system interface signal is not.  
If this pin is "H", LCD Module displays AGP (Auto Generation Pattern).



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Rear view of LCM



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### 3-3. Signal Timing Specifications

Table 4 shows the signal timing required at the input of the Vx1 transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

**Table 4. TIMING TABLE (DE Only Mode)**

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	$t_{HV}$	480	480	480	$t_{CLK}$	3840/8
	Blank	$t_{HB}$	60	70	120	$t_{CLK}$	1
	Total	$t_{HP}$	540	550	600	$t_{CLK}$	
Vertical	Display Period	$t_{VV}$	2160	2160	2160	Lines	
	Blank	$t_{VB}$	40	90	600	Lines	1
	Total	$t_{VP}$	2200	2250	2760	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	$f_{CLK}$	60	74.25	78.00	MHz	594/8
	Horizontal	$f_H$	121.8	135	140	KHz	2
	Vertical	$f_V$	47	60	63	Hz	2

notes: 1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode).  
If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.

2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency

3. Spread Spectrum Rate (SSR) is limited to  $\pm 0.5\%$  center spread at 30KHz

※ Timing should be set based on clock frequency.

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## 3-4. V by One Signal Specifications

## 3-4-1. V by One input Signal Timing Diagram

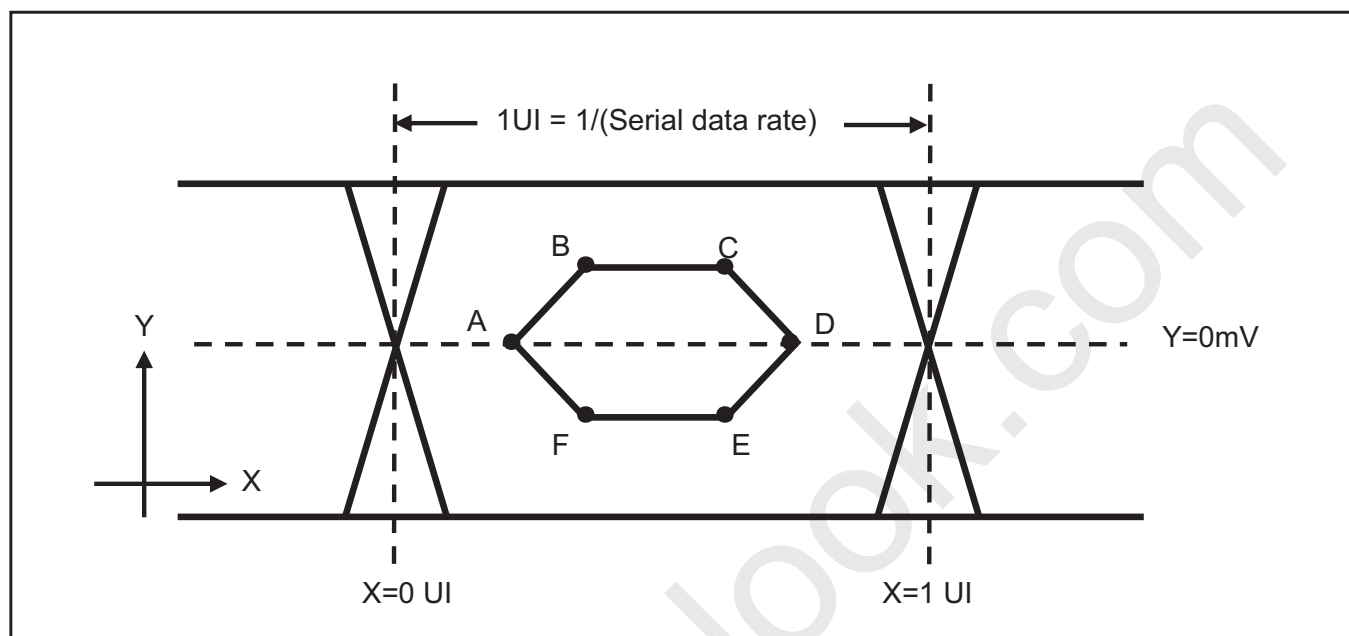


Table 5. Eye Mask Specification

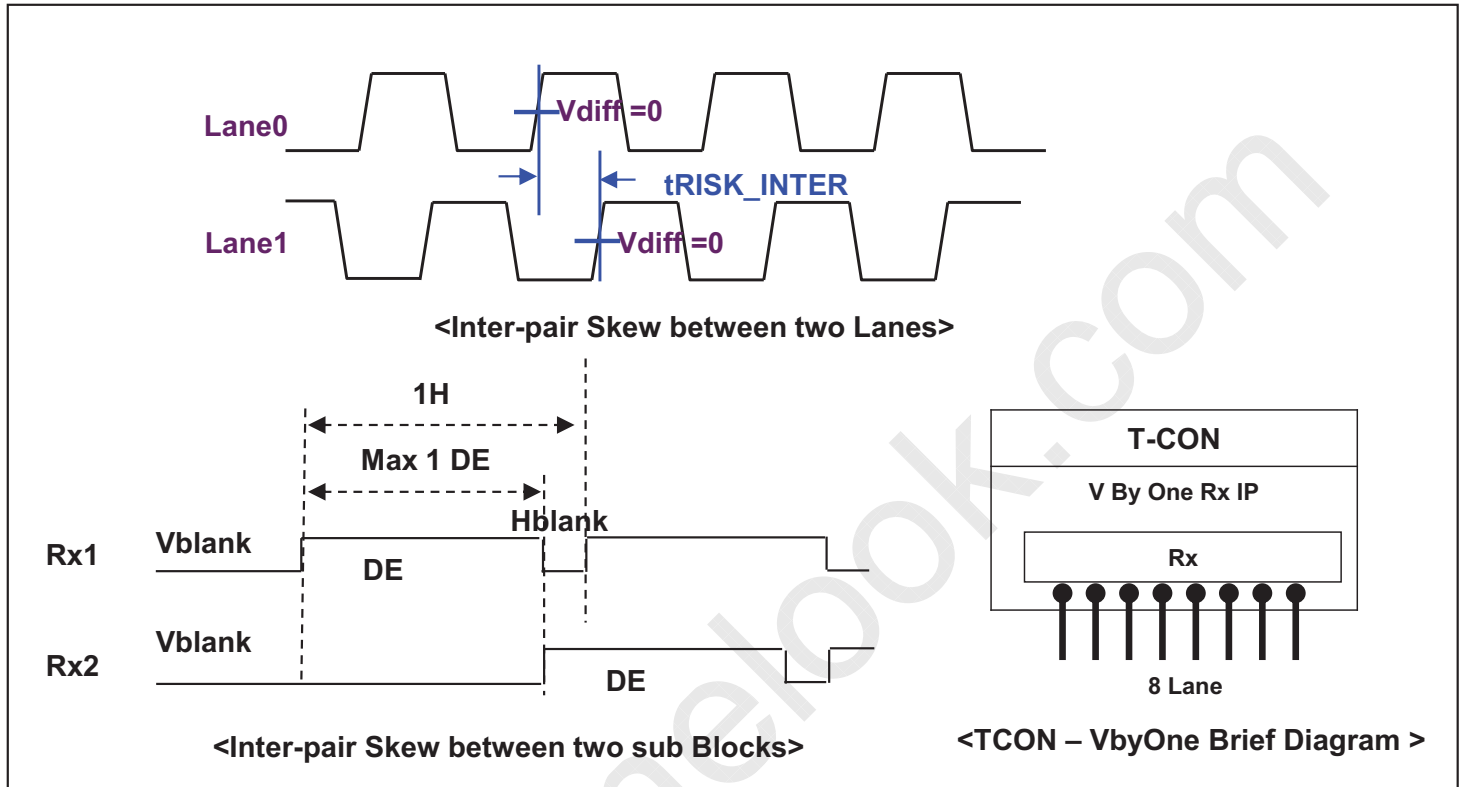
	X[UI]	Note	Y[mV]	Note
A	0.25 (max)	2	0	-
B	0.3 (max)	2	50	3
C	0.7(min)	3	50	3
D	0.75(min)	3	0	-
E	0.7(min)	3	-50	3
F	0.3(max)	2	-50	3

- notes
1. All Input levels of V by One signals are based on the V by One HS Standard Ver. 1.4
  2. This is allowable maximum value.
  3. This is allowable minimum value.
  4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
    - PLL bandwidth : 15 Mhz
    - Damping Factor : 1

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## 3-4-2. V by One Input Signal Characteristics



Description	Symbol	Min	Max	Unit	notes
Allowable inter-pair skew between lanes	$t_{RISK\_INTER}$	-	5	UI	1,3
Allowable iner-pair skew between sub-blocks	$t_{RISK\_BLOCK}$	-	1	DE	1,4

## Notes 1.1UI = 1/serial data rate

2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.

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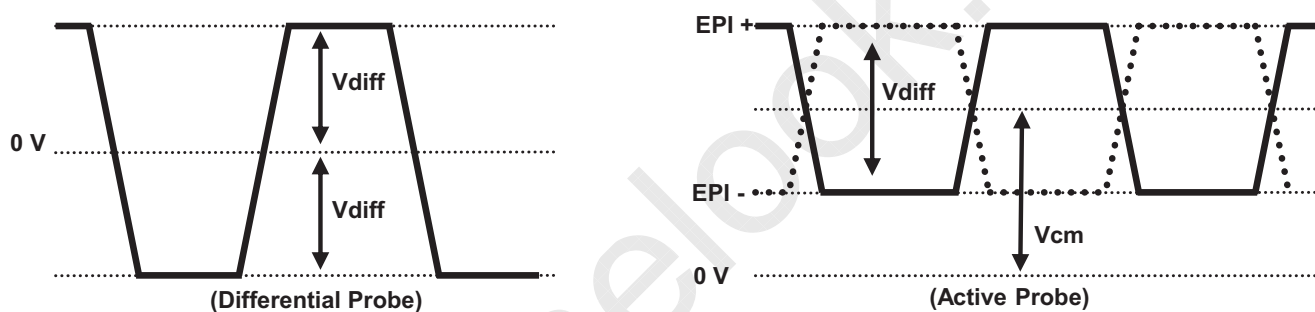
## Product Specification

## 3-5. Intra interface Signal Specification

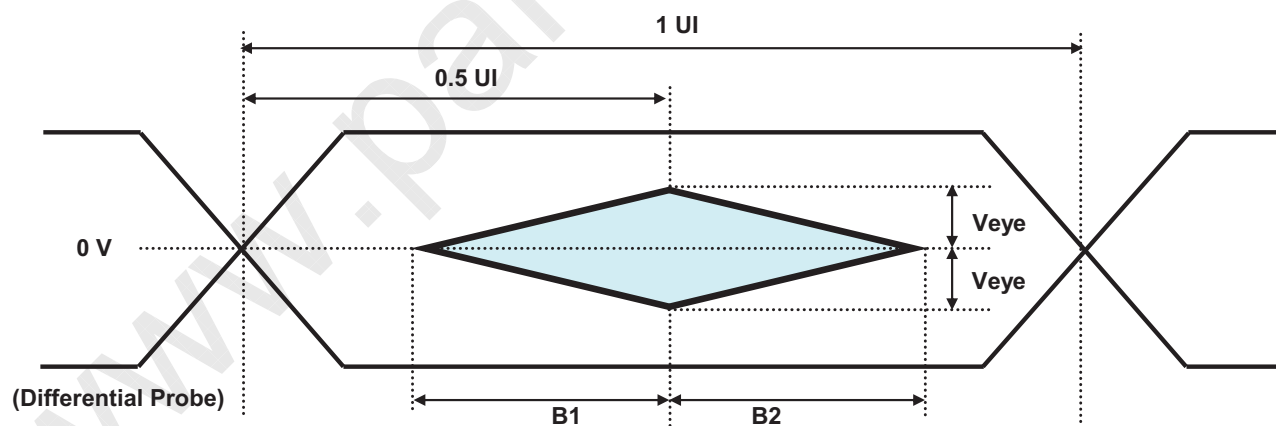
## 3-5-1. EPI Signal Specification

Table 6. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	notes
Logic & EPI Power Voltage	VCC	-	1.62	1.8	1.98	VDC	
EPI input common voltage	VCM	CML Type	0.8	-	$1.2 - V_{diff}/2$	V	
EPI input differential voltage	Vdiff	-	150	-	500	mV	
EPI Input eye diagram	Veye	-	90	-	-	mV	
Effective Veye width time	B1&B2		0.25	-	-	UI	



EPI Differential signal characteristics



Eye Pattern of EPI Input

\*Source PCB

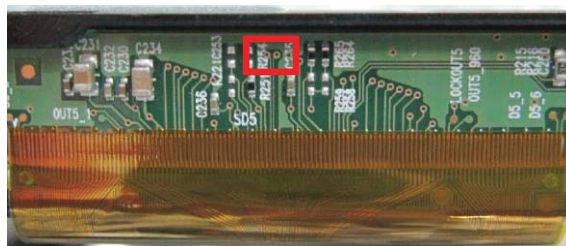


FIG. 1 Measure point



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### 3-6. Color Data Reference

The brightness of each primary color (red, green, blue) is based on the 10bit or 8bit gray scale data input for the color.

The higher binary input, the brighter the color. Table 7 provides a reference for color versus data input.

**Table 7. COLOR DATA REFERENCE**

Packer input & Unpacker output		30bpp RGB (10bit)	24bpp RGB (8bit)
Byte0	D[0]	R[2]	R[0]
	D[1]	R[3]	R[1]
	D[2]	R[4]	R[2]
	D[3]	R[5]	R[3]
	D[4]	R[6]	R[4]
	D[5]	R[7]	R[5]
	D[6]	R[8]	R[6]
	D[7]	R[9]	R[7]
Byte1	D[8]	G[2]	G[0]
	D[9]	G[3]	G[1]
	D[10]	G[4]	G[2]
	D[11]	G[5]	G[3]
	D[12]	G[6]	G[4]
	D[13]	G[7]	G[5]
	D[14]	G[8]	G[6]
	D[15]	G[9]	G[7]
Byte2	D[16]	B[2]	B[0]
	D[17]	B[3]	B[1]
	D[18]	B[4]	B[2]
	D[19]	B[5]	B[3]
	D[20]	B[6]	B[4]
	D[21]	B[7]	B[5]
	D[22]	B[8]	B[6]
	D[23]	B[9]	B[7]
Byte4	D[24]	Don't care	
	D[25]	Don't care	
	D[26]	B[0]	
	D[27]	B[1]	
	D[28]	G[0]	
	D[29]	G[1]	
	D[30]	R[0]	
	D[31]	R[1]	

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## 3-7. Power Sequence

## 3-7-1. LCD Driving circuit

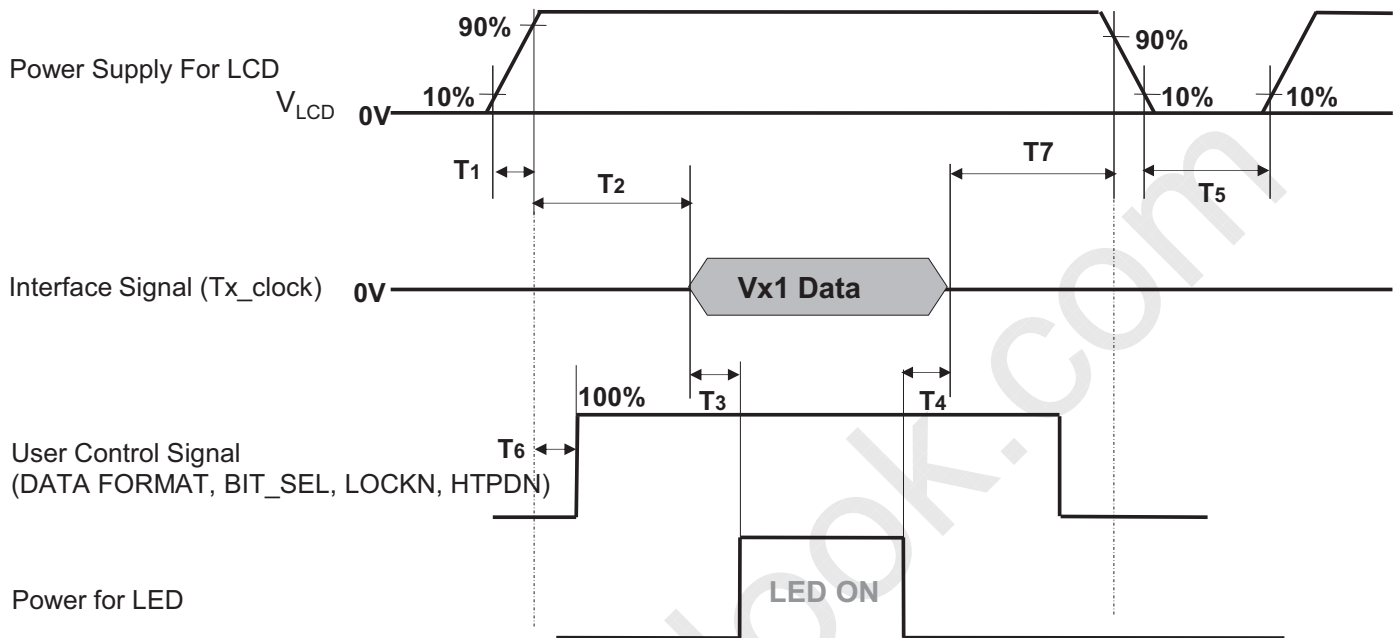


Table 8. POWER SEQUENCE

Parameter	Value			Unit	Note
	Min	Typ	Max		
T1	0.5	-	20	ms	1
T2	0	-	-	ms	2
T3	400	-	-	ms	3
T4	100	-	-	ms	3
T5	3.0	-	-	s	4
T6	0	-	T2	ms	5
T7	0	-	-	ms	6

- note :
1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.
  2. If T2 is satisfied with specification after removing LVDS Cable, there is no problem.
  3. The T3 / T4 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.
  4. T5 should be measured after the Module has been fully discharged between power off and on period.
  5. If the on time of signals (Interface signal and user control signals) precedes the on time of Power ( $V_{LCD}$ ), it will be happened abnormal display. When T6 is NC status, T6 doesn't need to be measured.
  6. It is recommendation specification that T7 has to be 0ms as a minimum value.
- ※ Please avoid floating state of interface signal at invalid period.  
※ When the power supply for LCD ( $V_{LCD}$ ) is off, be sure to pull down the valid and invalid data to 0V.

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## 4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at  $25\pm 2^{\circ}\text{C}$ . The values are specified at 50cm from the LCD surface at a viewing angle of  $\Phi$  and  $\theta$  equal to  $0^{\circ}$ .

FIG. 2 shows additional information concerning the measurement equipment and method.

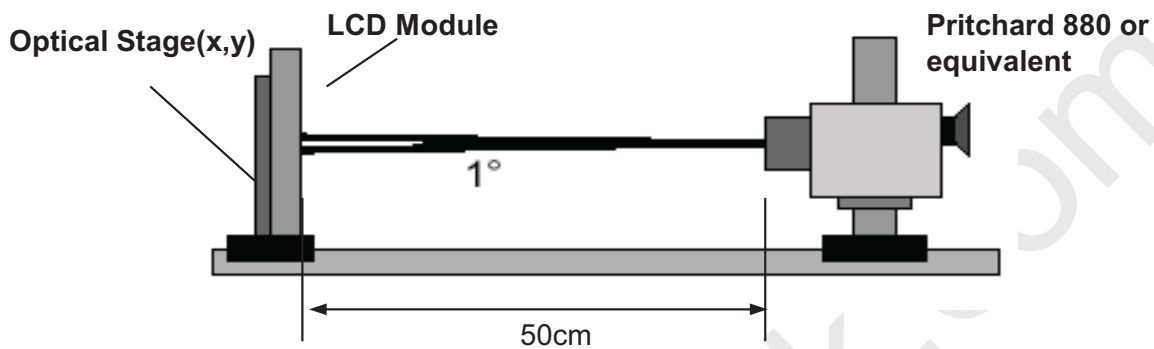


FIG. 2 Optical Characteristic Measurement Equipment and Method

$T_a = 25\pm 2^{\circ}\text{C}$ ,  $V_{\text{LCD}} = 12.0\text{V}$ ,  $f_v = 60\text{Hz}$ ,  $D_{\text{clk}} = 74.25\text{MHz}$ ,  
Light Source : D65 Standard

Table 9. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	800	1100 (TBD)	-		1
Response Time	Gray to Gray	G to G	-	8 (TBD)	12 (TBD)	ms	2
	Uniformity	$\delta_{\text{G TO G}}$	-	-	1		3
Transmittance		T	4.87 (TBD)	5.42 (TBD)		%	4
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.662 (TBD)	Typ +0.03		5
		Ry		0.329 (TBD)			
	GREEN	Gx		0.270 (TBD)			
		Gy		0.575 (TBD)			
	BLUE	Bx		0.135 (TBD)			
		By		0.110 (TBD)			
Viewing Angle (CR>10)							
	x axis, right( $\phi=0^{\circ}$ )	$\theta_r$	89	-	-	degree	6
	x axis, left ( $\phi=180^{\circ}$ )	$\theta_l$	89	-	-		
	y axis, up ( $\phi=90^{\circ}$ )	$\theta_u$	89	-	-		
	y axis, down ( $\phi=270^{\circ}$ )	$\theta_d$	89	-	-		
Gray Scale			-	-	-		7



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note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

The value of CR should be extracted using the LGD sheet structure (Diffuser/Prism/Prism)

2. Response time is the time required for the display to transit from Gray(N) to Gray(M) (Rise Time,  $Tr_R$ ) and from Gray(M) to Gray(N) (Decay time,  $Tr_D$ ). For additional information see the FIG. 3.

※ G to G Spec stands for average value of all measured points.

Photo Detector : RD-80S / Field : 2 °

The response time is valued with operating condition of LGD's standard BLU

3. The variation of G to G Uniformity ,  $\delta$  G to G is defined as :

$$\text{G to G Uniformity} = \frac{\text{Maximum (GtoG)} - \text{Typical(GtoG)}}{\text{Typical(GtoG)}} \leq 1$$

\*Maximum(G to G) means maximum value of measured time(N,M = 0(Black)~1023(White), 128 gray step).

4. The value of transmittance should be extracted using the LGD standard sheet structure Diffuser/Diffuser)

5. The value of color coordinates should be extracted using the standard light source of D65

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 4.

7. Gray scale specification

Gamma Value is approximately 2.2. For more information, see the Table 10.

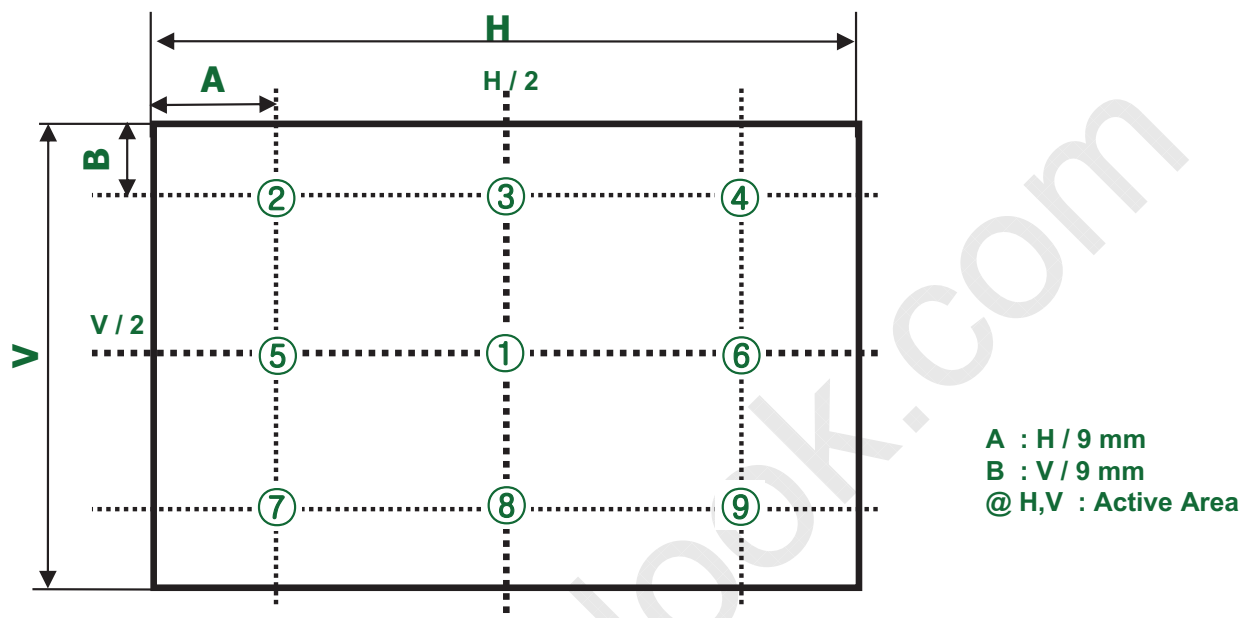
**Table 10. GRAY SCALE SPECIFICATION**

Gray Level	Luminance [%] (Typ)
L0	0.45
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

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Measuring point for surface luminance & measuring point for luminance variation.



Response time is defined as the following figure and shall be measured by switching the input signal for “Gray(N)” and “Gray(M)”.

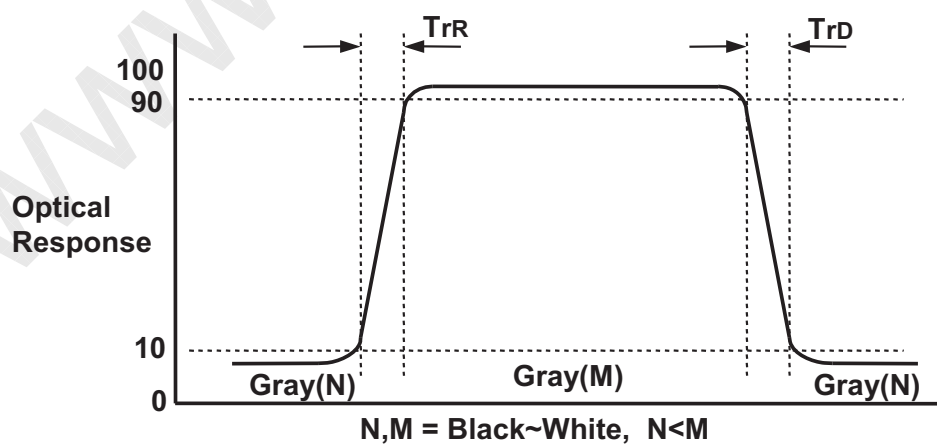


FIG. 3 Response Time

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## Dimension of viewing angle range

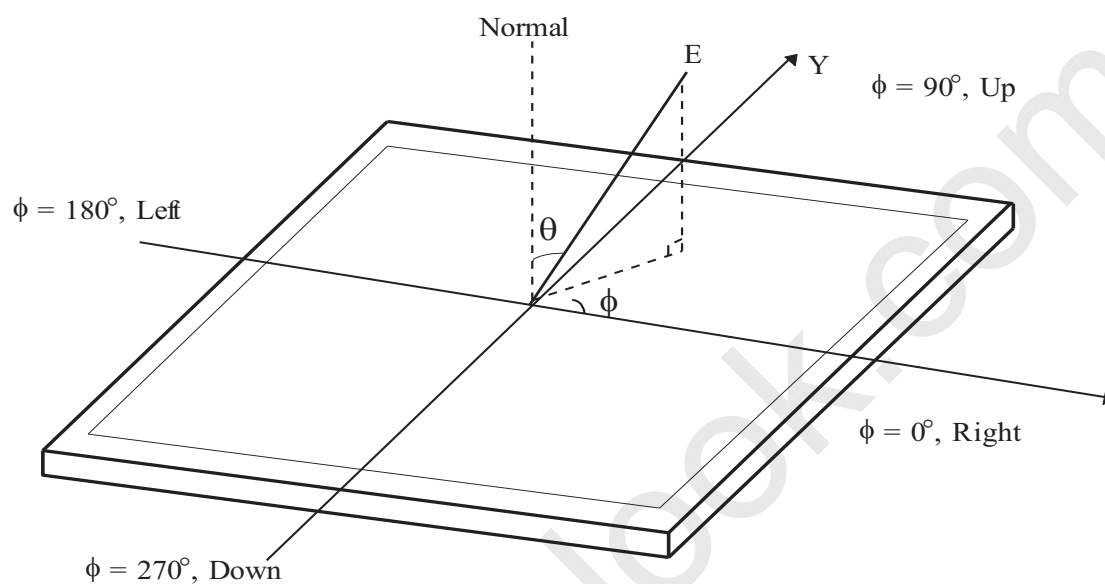


FIG. 4 Viewing Angle

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## 5. Mechanical Characteristics

Table 11 provides general mechanical characteristics.

**Table 11. MECHANICAL CHARACTERISTICS**

Item	Value	
Outline Dimension (Only Glass)	Horizontal	1913.0mm
	Vertical	1084.0mm
	Thickness	1.3mm
Active Display Area	Horizontal	1895.04mm
	Vertical	1065.96mm
Weight	5.9 kg(Typ.), 6.2 kg(Max)	
Surface Treatment	Hard coating(2H), Anti-glare low reflection treatment of the front polarizer (Haze 28%(Typ.))	

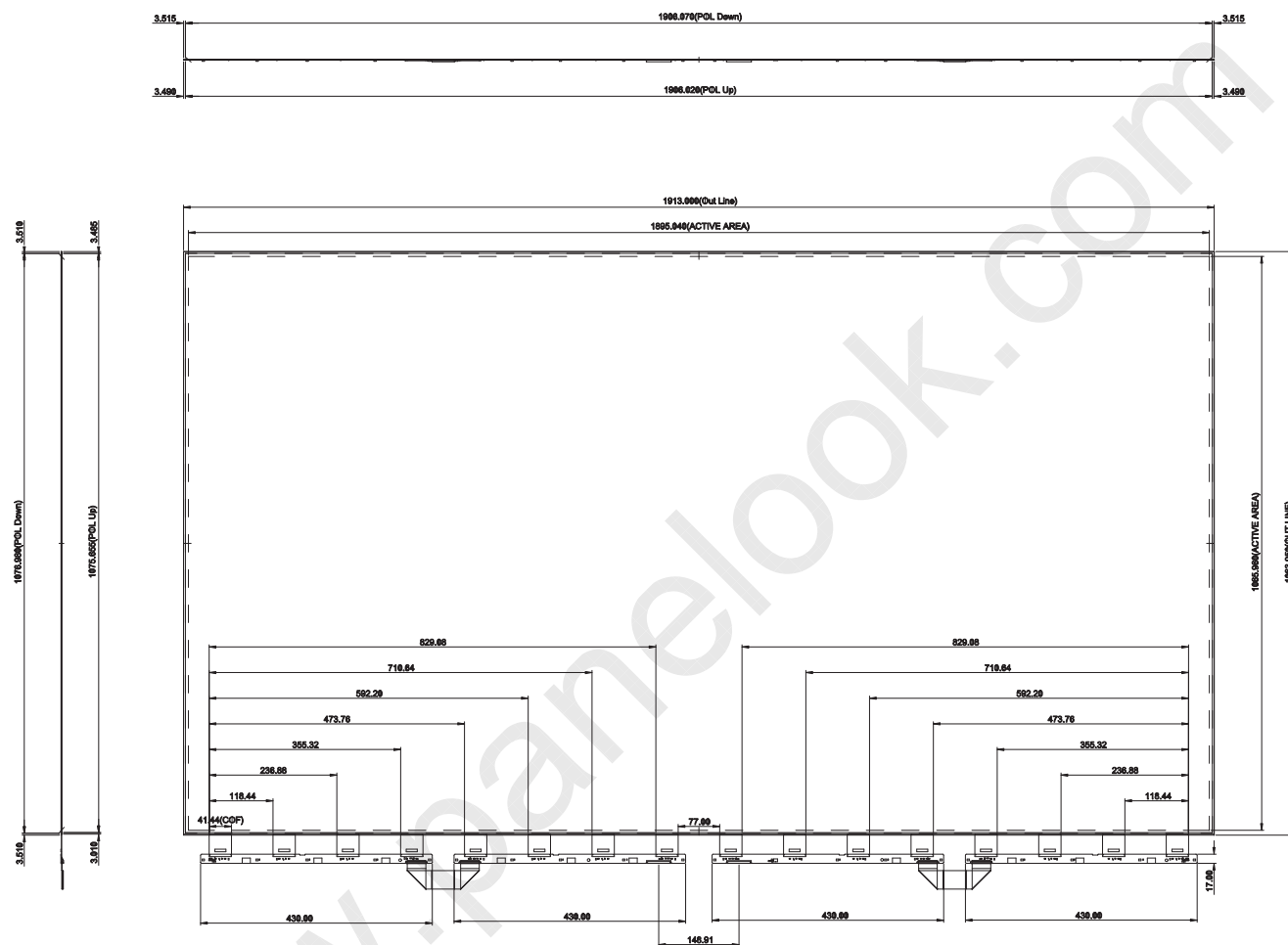
note : Please refer to a mechanical drawing in terms of tolerance at the next page.

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## 6. Mechanical Dimension

## 6-1. Board Assembly Dimension



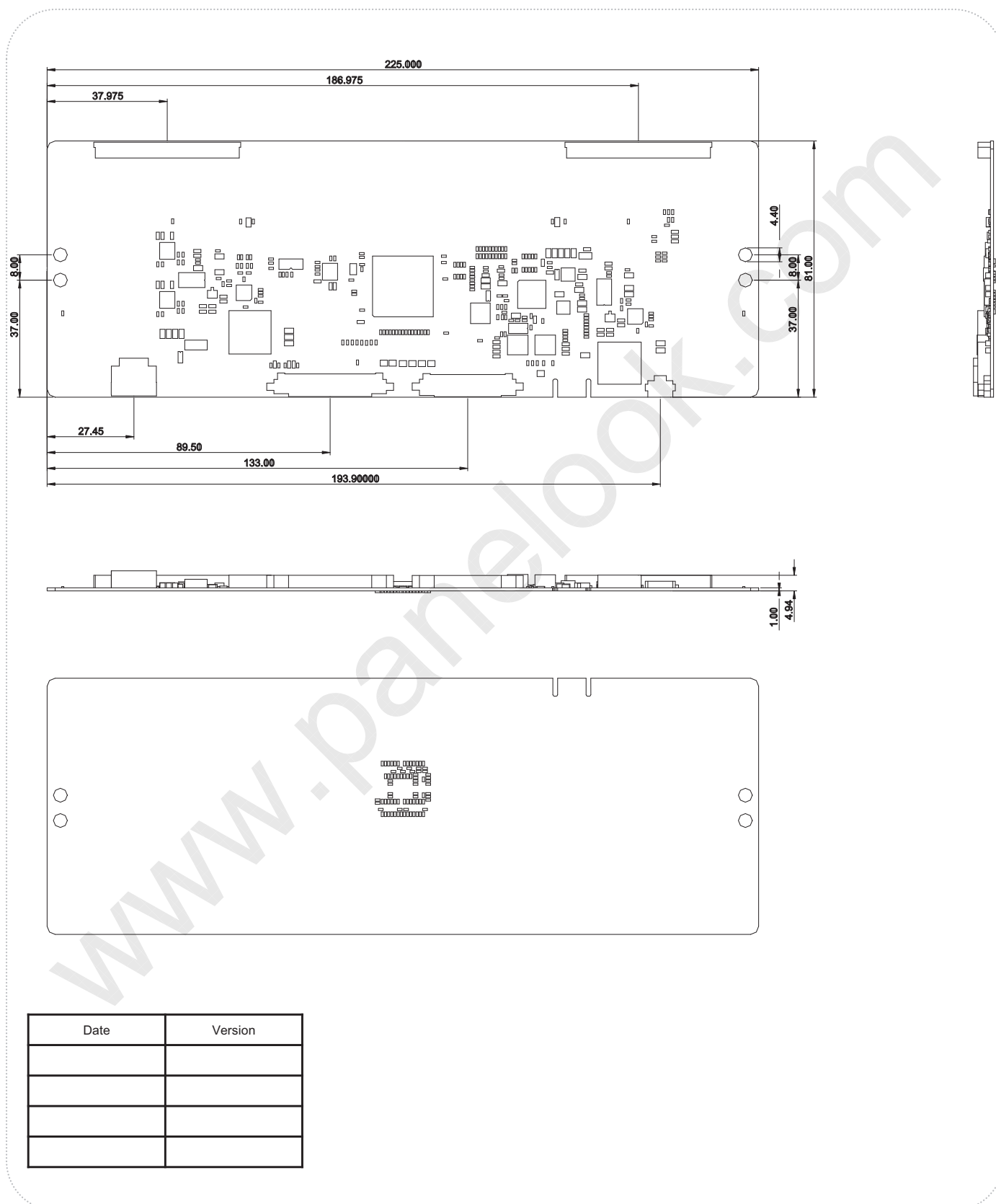
Notes  
1. This drawing describes how to assembly panel, pcb assy and COF.  
2. See part drawings for more detailed dimension.  
3. Polarize size are:  
Upper polarizer: 1998.020 \* 1975.000  
Lower polarizer: 1998.070 \* 1975.000

Date	Version

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## Product Specification

## 6-2. Control Board Assembly Dimension





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## Product Specification

## 7. Reliability

**Table 12. ENVIRONMENT TEST CONDITION**

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 90% 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 500h
4	Low temperature operation test	Ta= 0°C 500h
5	Humidity condition Operation	Ta= 40 °C ,90%RH
6	Altitude      operating storage / shipment	0 - 16,400 ft 0 - 40,000 ft

note : 1. Before and after Reliability test, LCM should be operated with normal function.

2. These conditions are for LGD's internal test. Please refer to Absolute Maximum Ratings (Table1) for guaranteed condition.



## Product Specification

## 8. International Standards

### 8-1. Safety

- a) UL 60065, Underwriters Laboratories Inc.  
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.  
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- c) IEC 60065, The International Electrotechnical Commission (IEC).  
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

### 8-2. Environment

- a) RoHS, Directive **2011/65/EU** of the European Parliament and of the council of **8 June 2011**



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## Product Specification

## 9. Packing

### 9-1. Information of B/Ass'y Label

#### a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M
---	---	---	---	---	---	---	---	---	---	---	---	---

A,B,C : SIZE(INCH)

E : MONTH

D : YEAR

F ~ M : SERIAL NO.

#### notes

##### 1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

##### 2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

#### b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the frontside of the Left Source PCB.  
This is subject to change without prior notice.

### 9-2. Packing Form

a) Package quantity in one Pallet : 60 pcs

b) Pallet Size : 2280 mm(W) X 1420 mm(D) X 950 mm(H)

## Product Specification

## 10. Precautions

Please pay attention to the followings when you use this TFT LCD module.

### 10-1. Handling Precautions

- (1) Please attach the surface transparent protective film to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (2) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (4) After removing the protective film, when the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaked with petroleum benzene. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (5) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (6) Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.
- (7) Please make sure to avoid external forces applied to the Source PCB and D-IC during the process of handling or assembling the TV set. If not, it causes panel damage or malfunction.
- (8) Panel and BLU should be protected from the static electricity. If not, it causes IC damage.
- (9) Do not pull or fold the source D-IC which connect the source PCB and the panel.
- (10) Panel (board ass'y) should be put on the BLU structure precisely to avoid mechanical impact.
- (11) FFC Cable should be connected between System board and Source PCB correctly.
- (12) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.
- (13) Surface temperature of the Source D-IC & Component on PCB should be controlled under 100°C with TV Set status.  
If not, problems such as IC damage or decrease of lifetime could occur.

### 10-2. Operating Precautions

- (1) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (2) Brightness depends on the temperature. (In lower temperature, it becomes lower.)  
And in lower temperature, Stable time (required time that brightness is stable after turned on) becomes longer
- (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

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## Product Specification

## 10-3. Protection Film

- (1) Please keep attaching the protection film before assembly.
- (2) Please peel off the protection film slowly.
- (3) Please peel off the protection film just like shown in the Fig. 5
- (4) Ionized air should be blown over during the peeling.
- (5) Source PCB should be connected to the ground when peel off the protection film.
- (6) The protection film should not be contacted to the source D-IC during peeling it off.

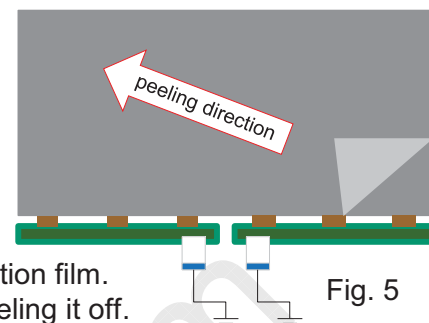


Fig. 5

## 10-4. Storage Precautions

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Temperature : 5 ~ 40 °C
- (2) Humidity : 35 ~ 75 %RH
- (3) Period : 6 months
- (4) Control of ventilation and temperature is necessary.
- (5) Please make sure to protect the product from strong light exposure, water or moisture. Be careful for condensation.
- (6) Please keep the modules at a circumstance shown below Fig. 6

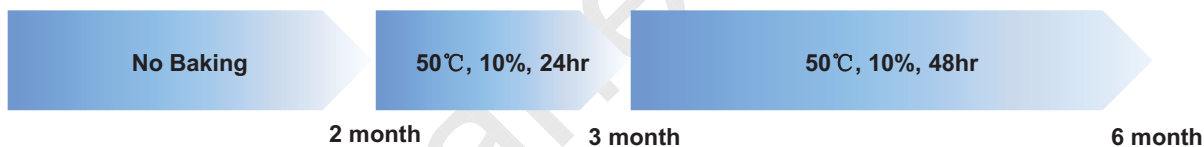


Fig. 6

## 10-5. Packing Precautions

Product assembled into module should be stored in the Al-bag(cover case).

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## Product Specification

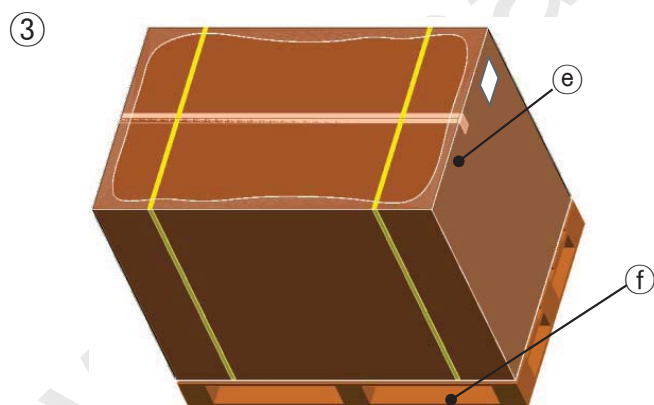
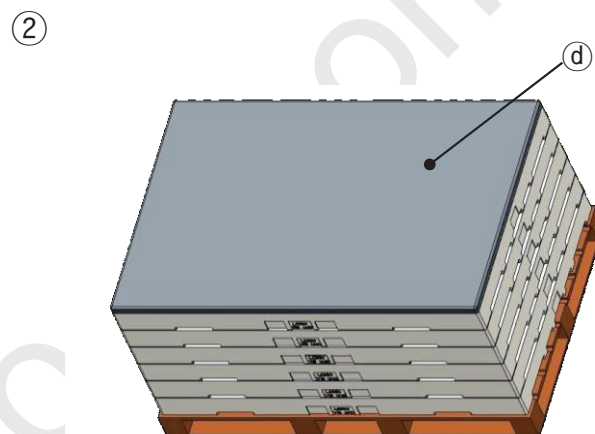
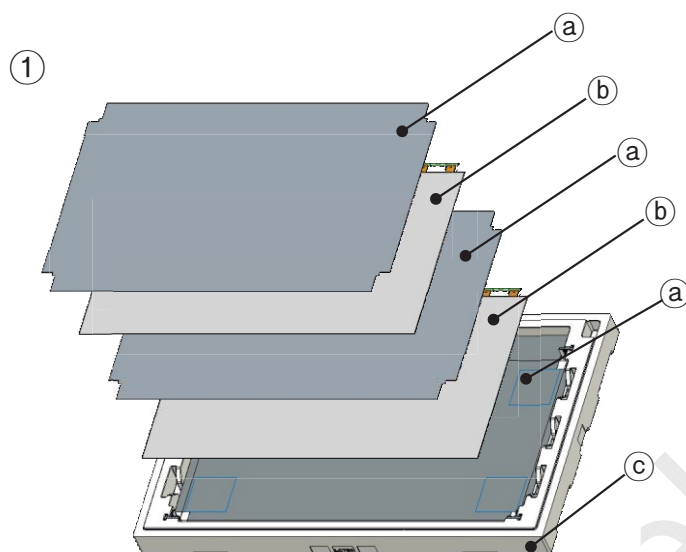
## # APPENDIX-I-1

## ■ Pallet Ass'y

a) B/Ass'y Qty + AL Cushion / Box : 12pcs + 13pcs

b) B/Ass'y Qty / Pallet : 60pcs

c) Box Qty / Pallet : 6Box



No.	Description	Material
(a)	AL Cushion	AL, PE
(b)	Board Ass'y	-
(c)	Bottom Packing	EPS
(d)	Top Packing	EPS
(e)	Angle Packing	Paper(SW)
(f)	Pallet	Plywood

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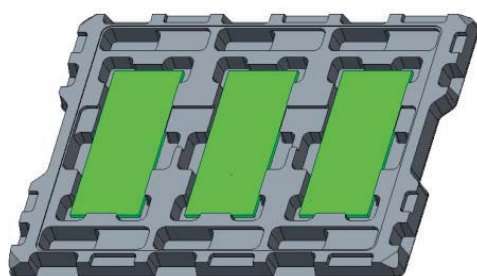
## Product Specification

## # APPENDIX-I-2

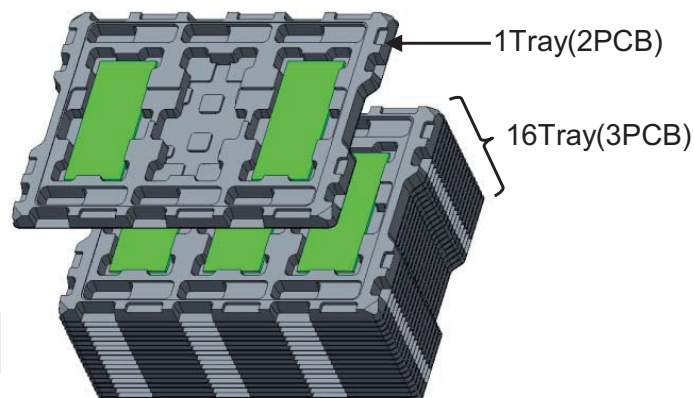
## ■ Control PCB Packing Ass'y

- a) Control PCB Q'ty / Box : 60 pcs
- b) Tray Q'ty / Box : 18Tray (16tray 3pcb, 1tray 2pcb, Top tray empty)
- c) Tray Size : 466 X 353 X 21.5
- d) Box size : 478 X 365 X 330

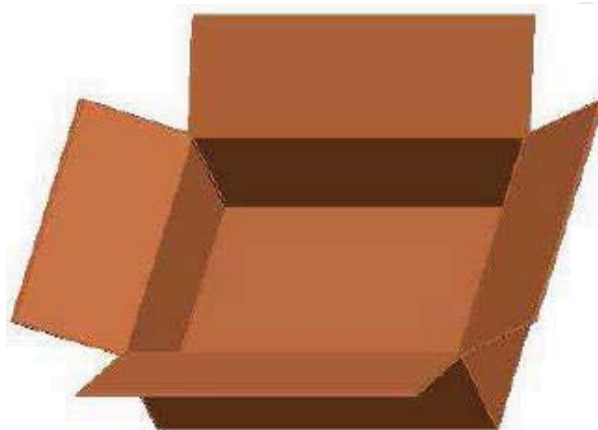
[ 3pcs/Tray ]



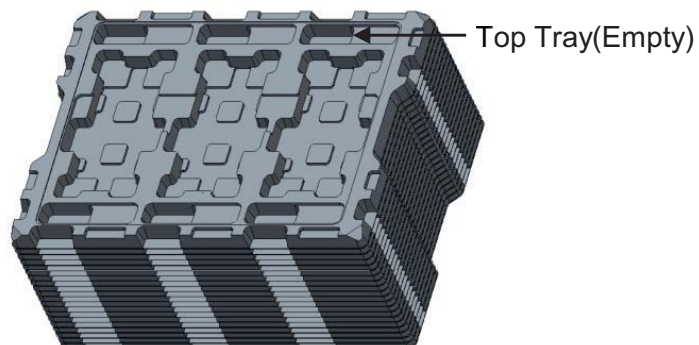
[ 17 Tray ]



[Inserting into Box]



[ 18 Tray ]



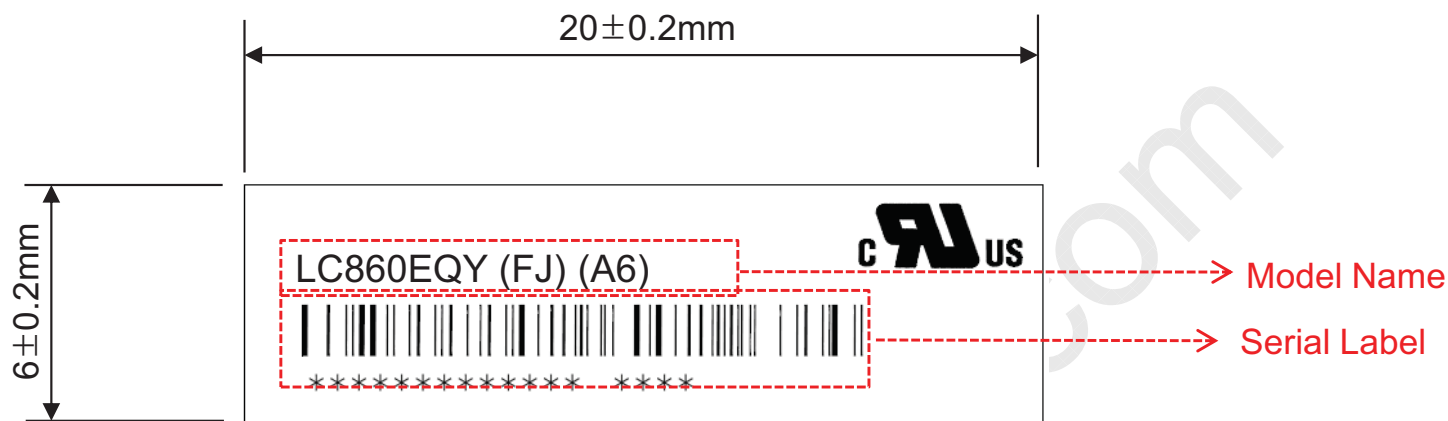
NO.	DESCRIPTION	MATERIAL
1	PCB Packing A,ssy	-
2	Tray	PET
3	Box	PAPER(SW)

LC860EQY

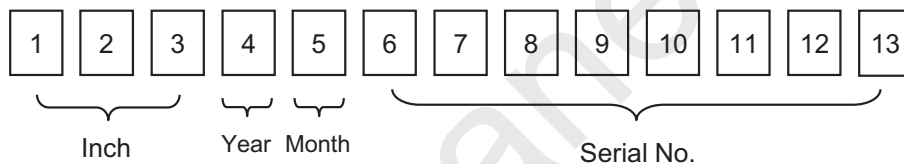
## Product Specification

## # APPENDIX-II-1

## ■ Serial Label



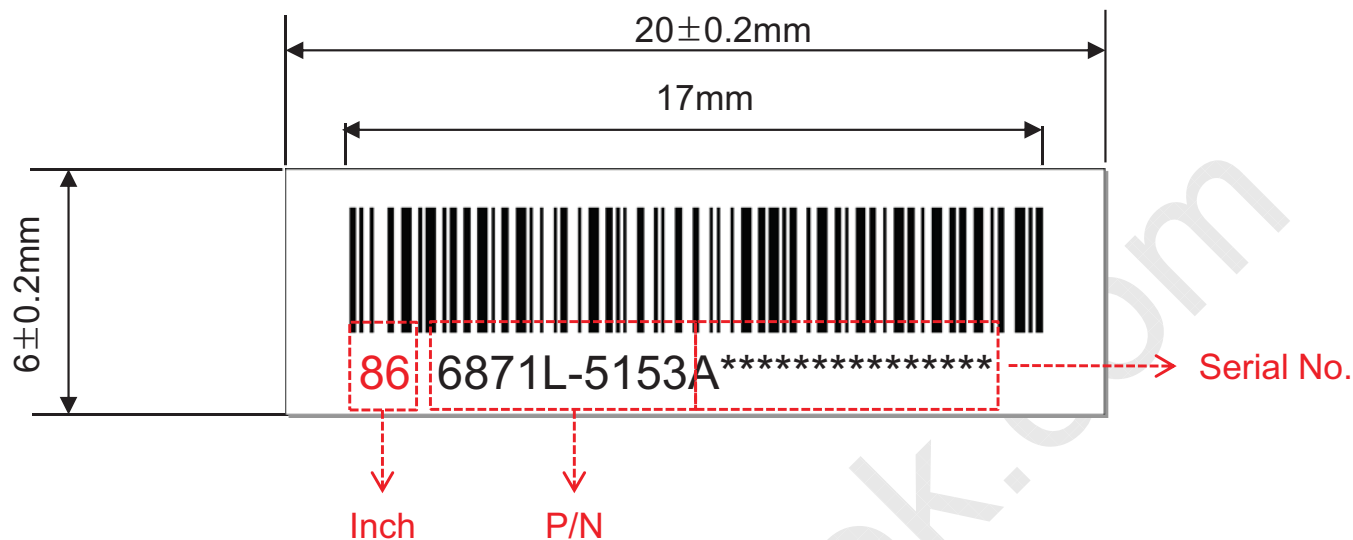
## ■ Serial No. (See CAS page 23 for more information)



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## Product Specification

## ■ Control PCB Label



## ■ Control PCB Box Label



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## Product Specification

## # APPENDIX-II-2

## ■ BOX Label



## ■ Pallet Label



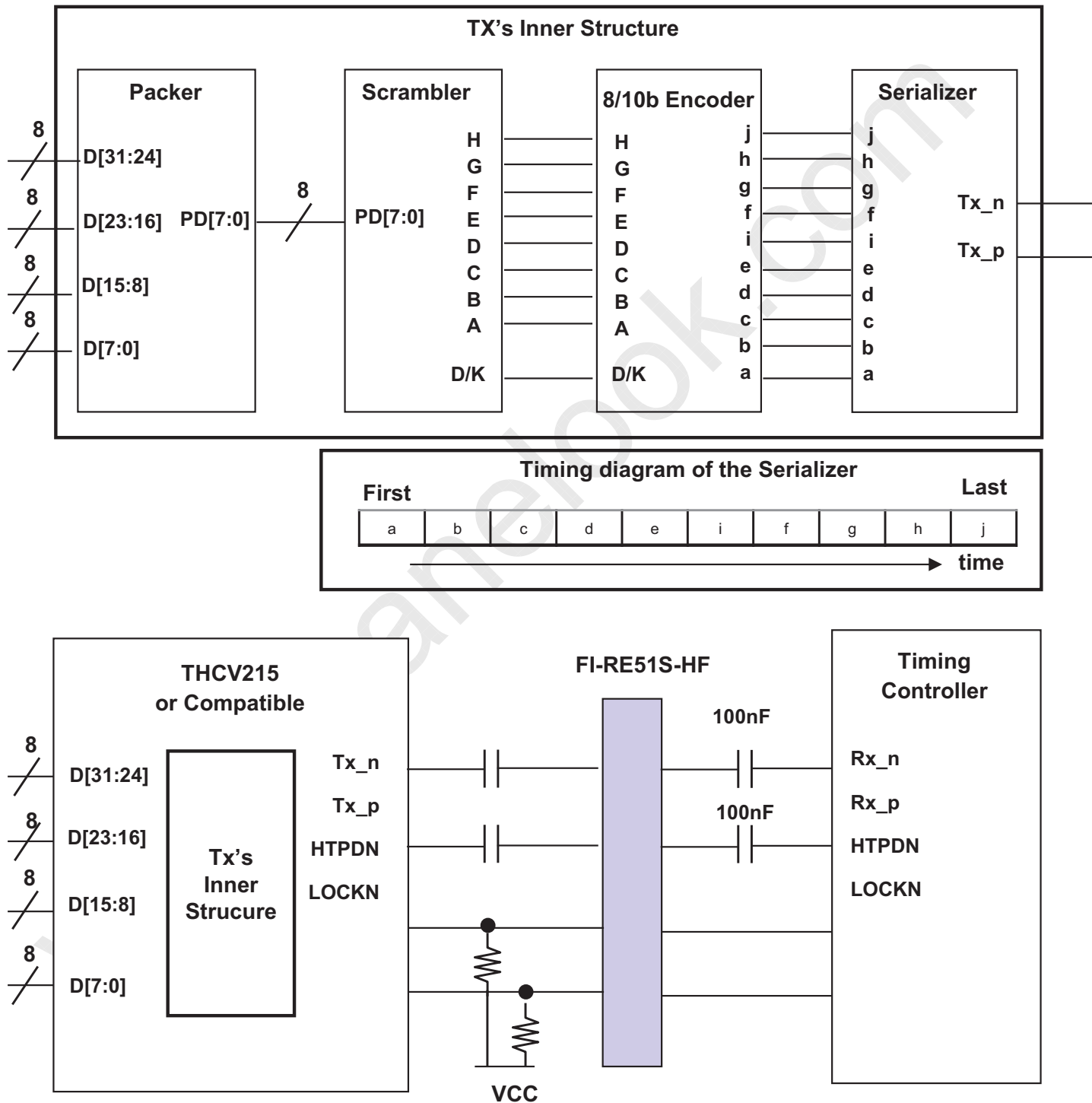


LC860EQY

## Product Specification

## # APPENDIX-III

## ■ Required signal assignment for Flat Link (Thine : THCV215) Transmitter



- notes: 1. The LCD module uses a 100 nF capacitor on positive and negative lines of each receiver input.  
 2. Refer to Vx1 Transmitter Data Sheet for detail descriptions. (THCV215 or Compatible)  
 3. About Module connector pin configuration, Please refer to the Page 8~9.

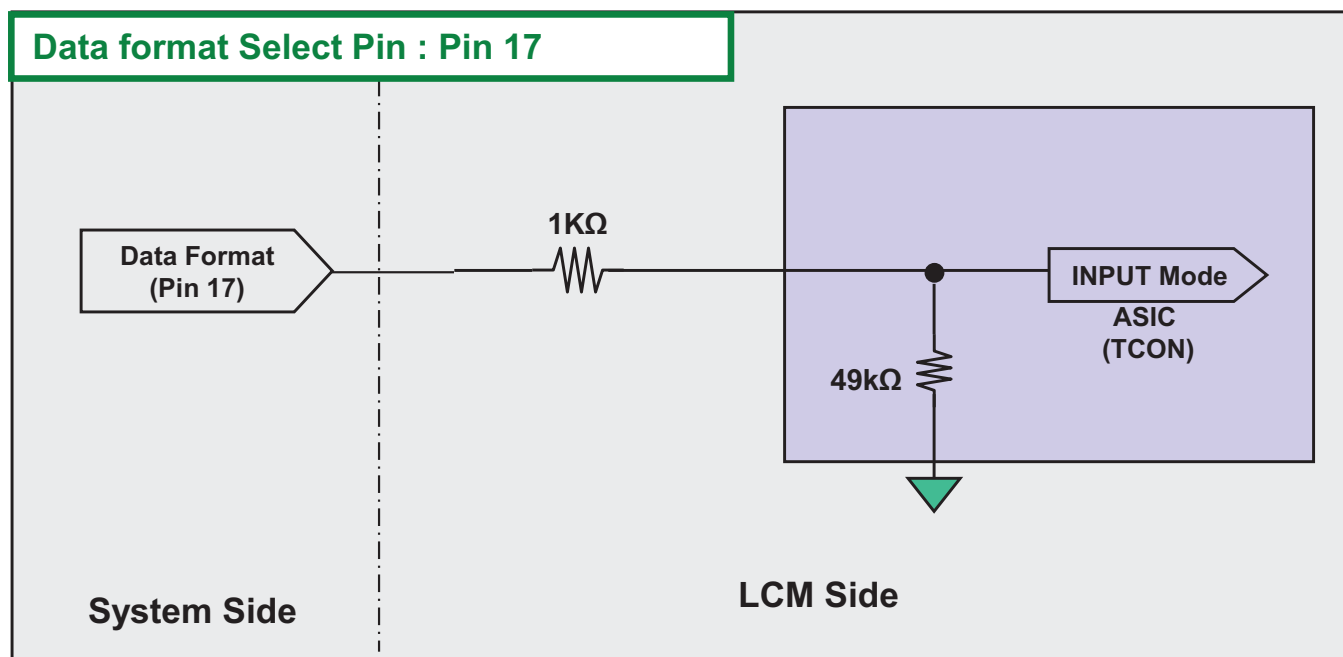
LC860EQY

## Product Specification

## # APPENDIX- IV-1

## ■ Option Pin Circuit Block Diagram

## 1) Circuit Block Diagram of Data format Selection pin



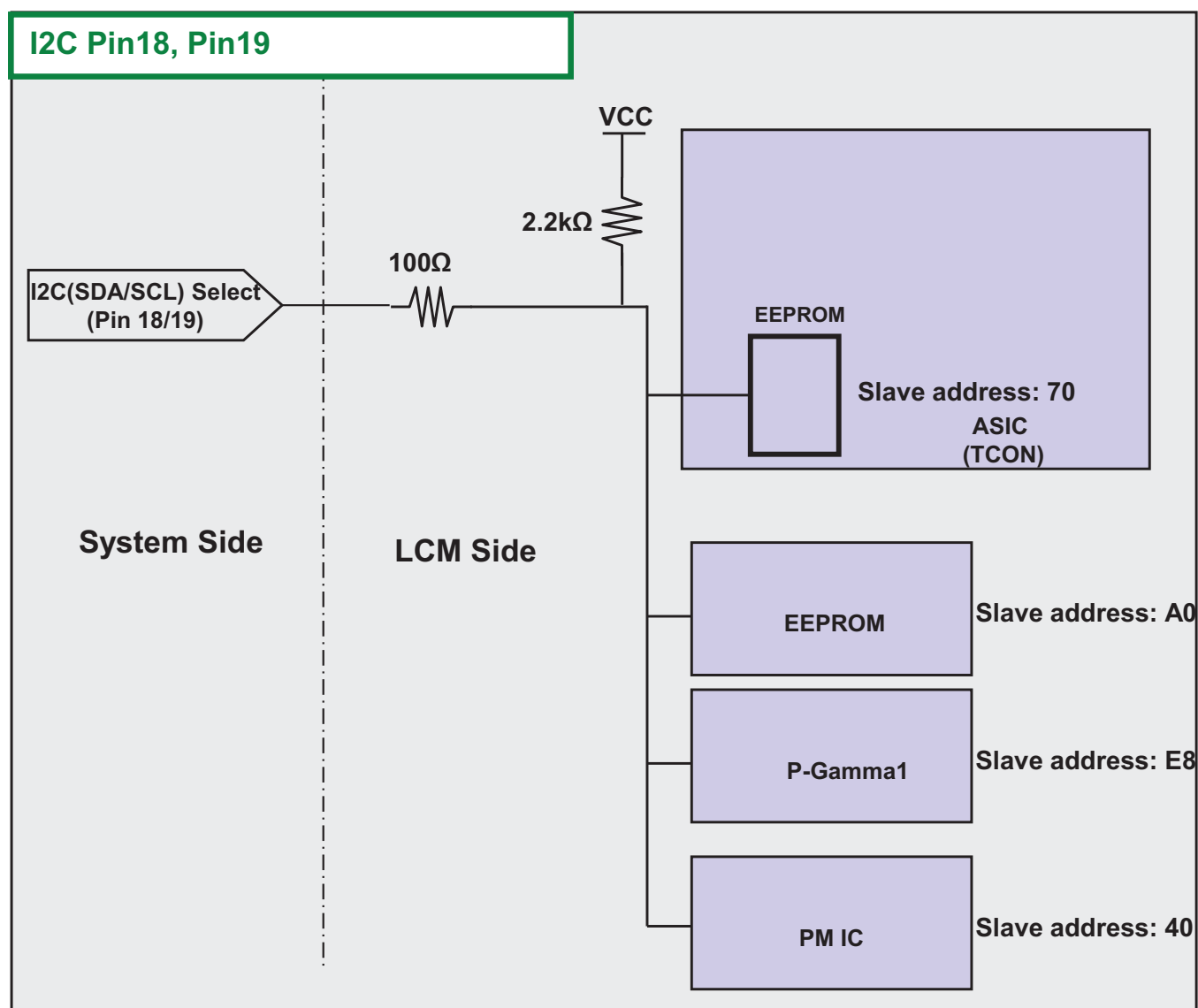
LC860EQY

## Product Specification

## # APPENDIX- IV-2

## ■ Option Pin Circuit Block Diagram

## 2) I2C(SDA/SCL) Selection pin



notes: 1. I2C Line of Set SoC avoid using slave address A0,E8,EA because LCD module uses those

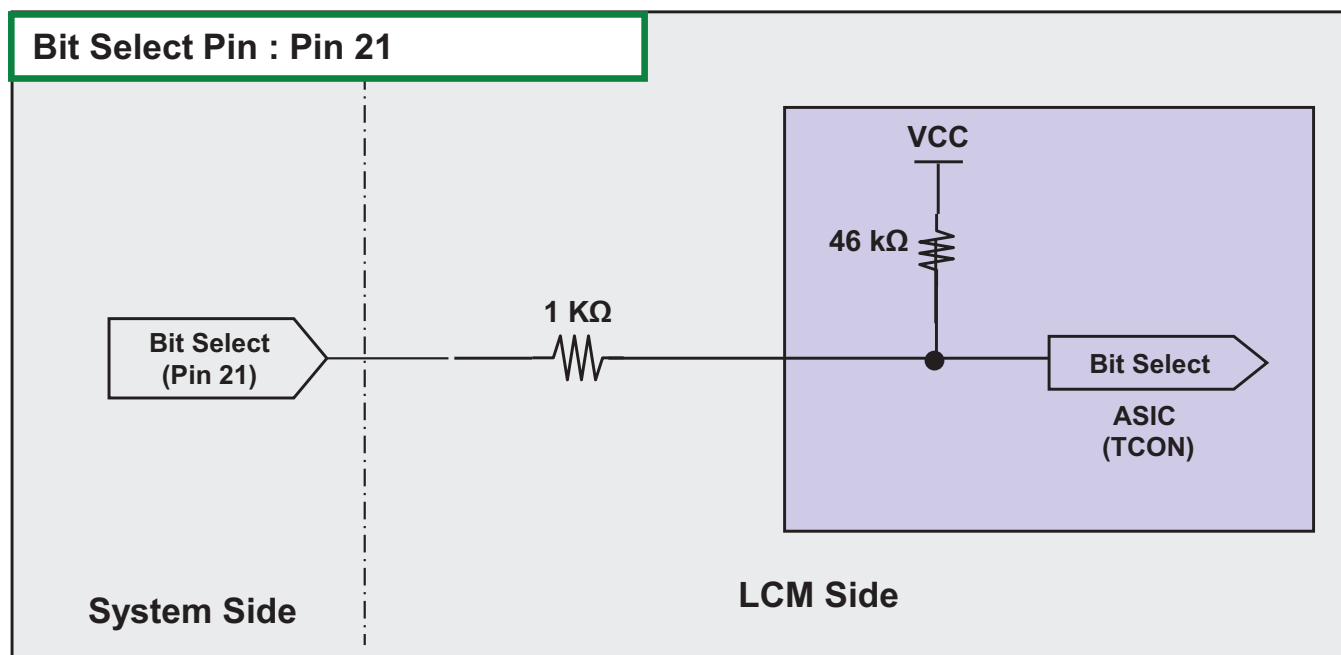
LC860EQY

## Product Specification

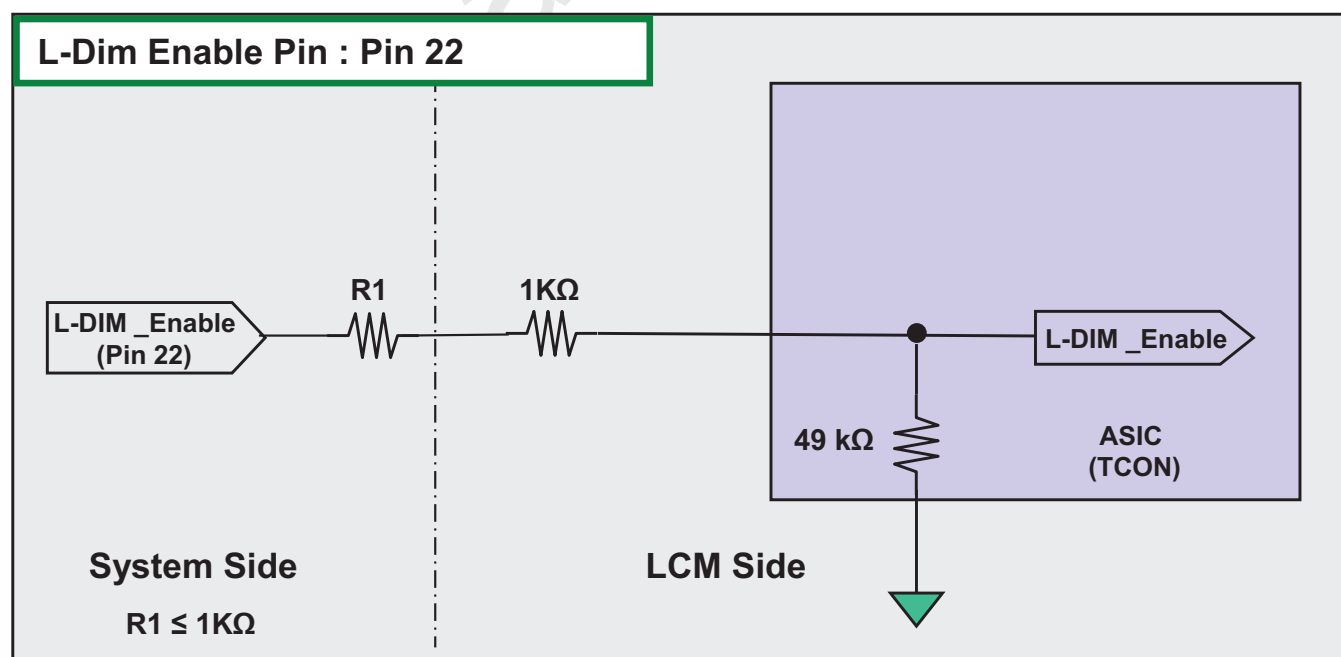
## # APPENDIX- IV-3

## ■ Option Pin Circuit Block Diagram

## 3) Circuit Block Diagram of Bit Selection pin



## 4) Circuit Block Diagram of L-Dim Enable Selection pin



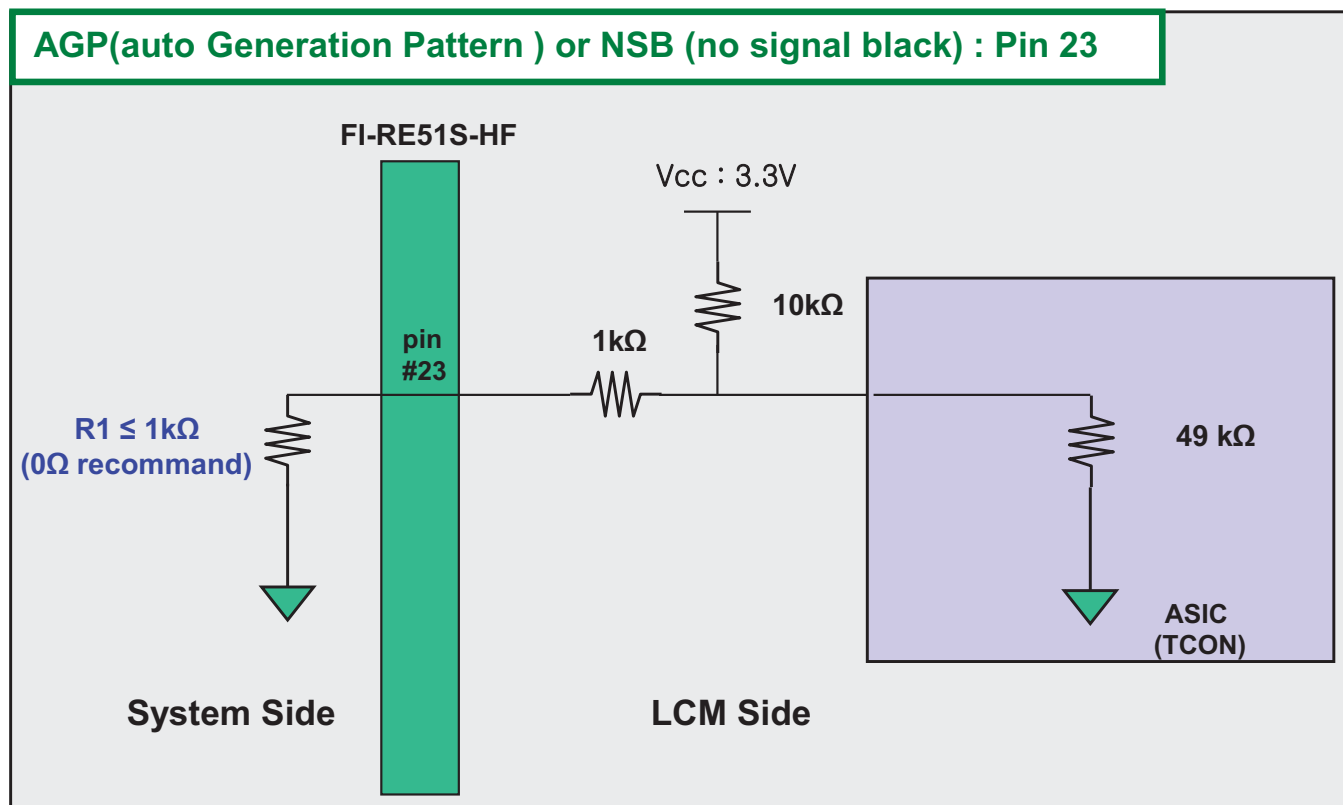
LC860EQY

## Product Specification

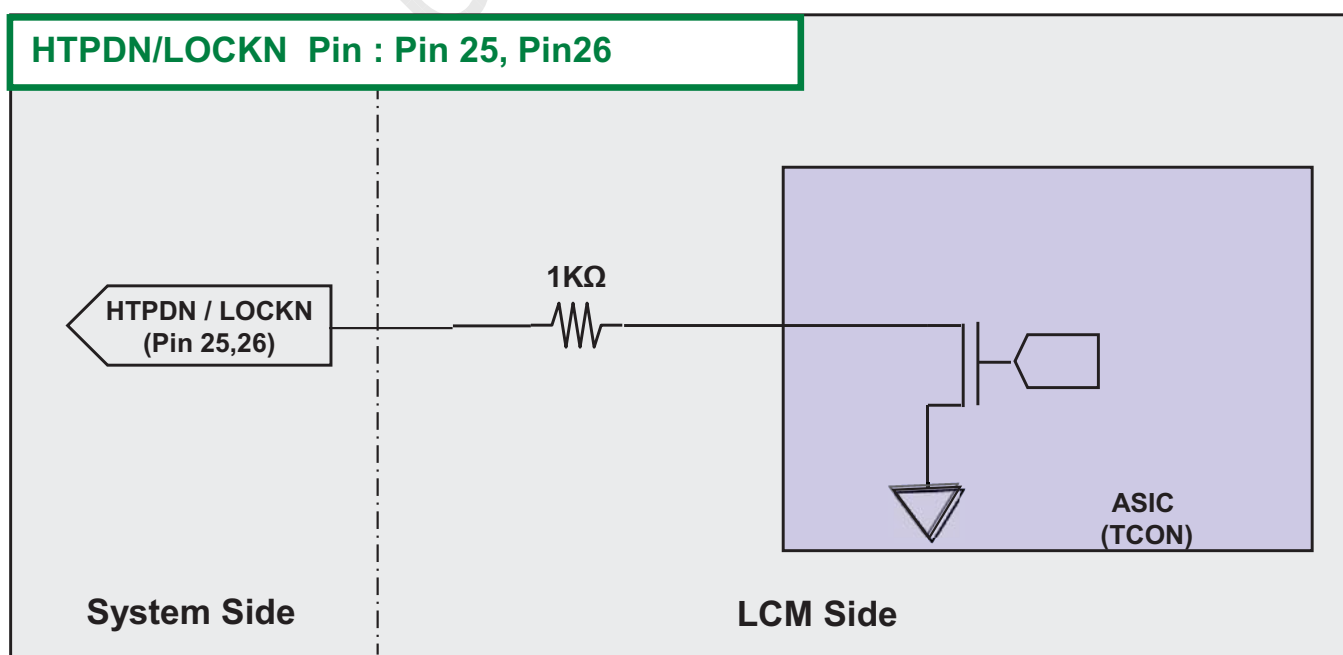
## # APPENDIX- IV-4

## ■ Option Pin Circuit Block Diagram

## 6) Circuit Block Diagram of AGP Selection pin



## 6) Circuit Block Diagram of HTPDN/ LOCKN Selection pin

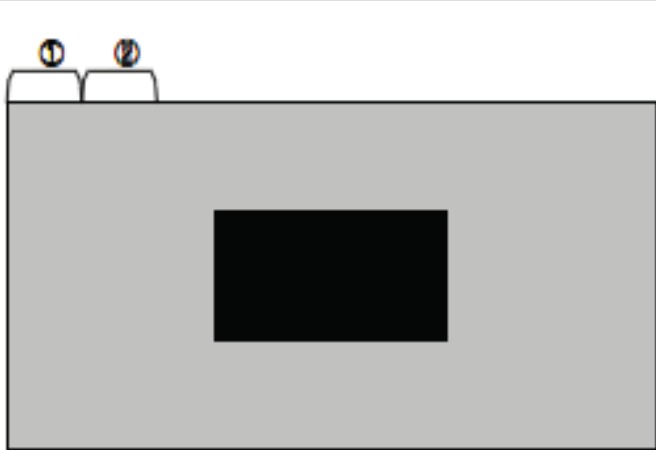
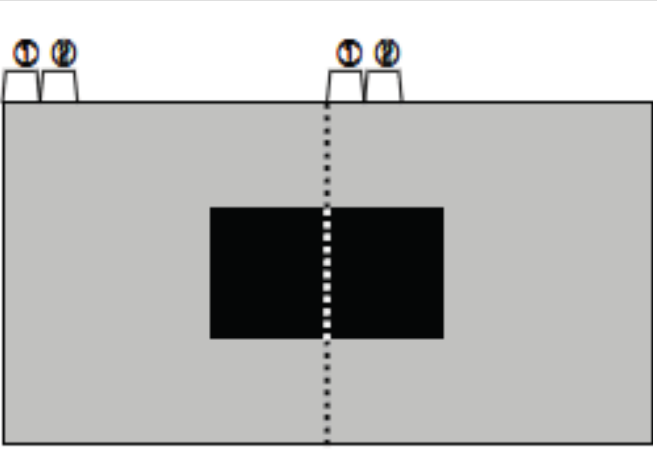


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## Product Specification

## # APPENDIX-V

## ■ input mode of pixel data

Mode 1 : Non-Division				Mode 2 : 2 Division			
							
Lane	1 <sup>st</sup> Data	2 <sup>nd</sup> Data	Data#	Lane	1 <sup>st</sup> Data	2 <sup>nd</sup> Data	Data#
Lane0	1	9	3833	Lane0	1	5	1917
Lane1	2	10	3834	Lane1	2	6	1918
Lane2	3	11	3835	Lane2	3	7	1919
Lane3	4	12	3836	Lane3	4	8	1920
Lane4	5	13	3837	Lane4	1921	1925	3837
Lane5	6	14	3838	Lane5	1922	1926	3838
Lane6	7	15	3839	Lane6	1923	1927	3839
Lane7	8	16	3840	Lane7	1924	1928	3840



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## Product Specification

## # APPENDIX-VI

## ■ The reference method of BL dimming

It is recommended to use synchronous V-sync frequency to prevent waterfall  
(Vsync \* 2 =P-Dim Frequency)

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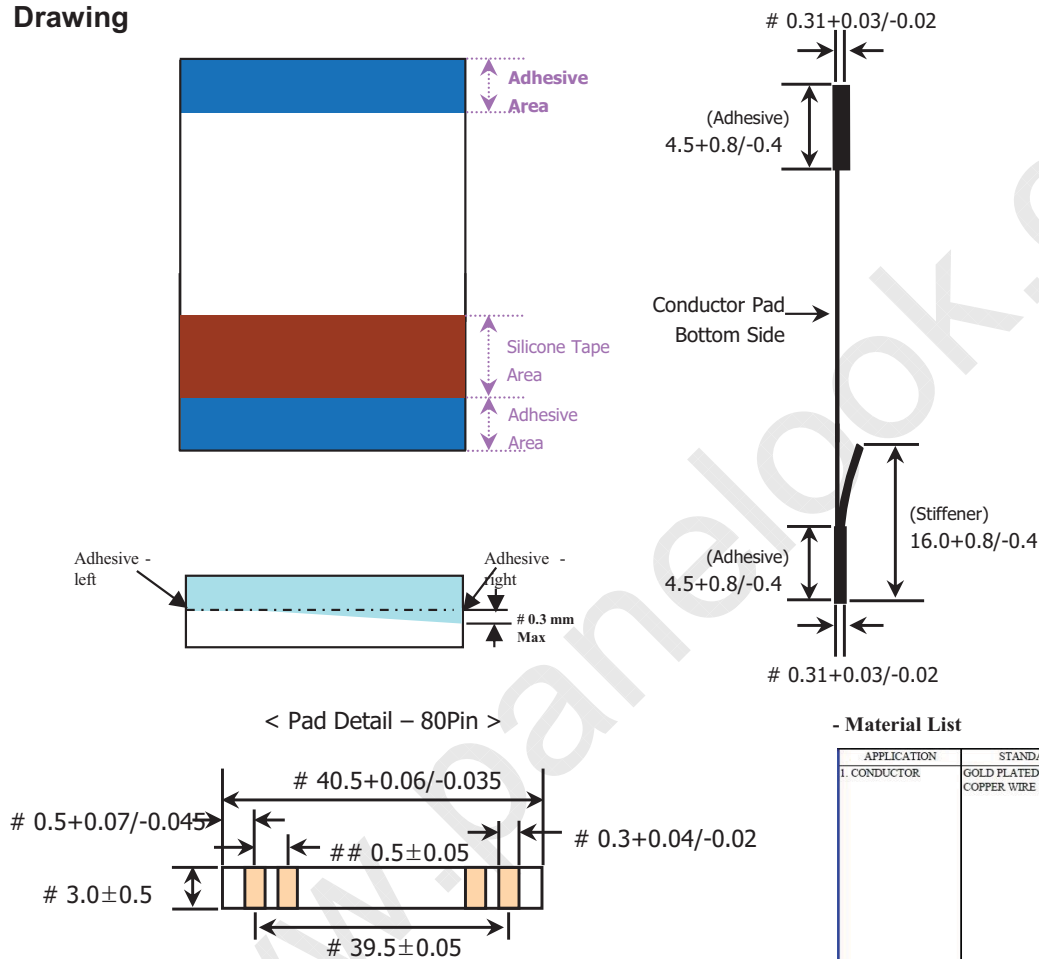
## Product Specification

## # APPENDIX-VII

## ■ FFC INFORMATION (LCD Connector )

- S-PCB : TF06L-80S-0.5SH (manufactured by HIROSE)
- C-PCB : TF06L-60S-0.5SH (manufactured by HIROSE)

## ■ Drawing



&lt; Pad Detail – 80Pin &gt;

## - Material List

APPLICATION	STANDARD	MATERIAL	REFERENCE
1. CONDUCTOR	GOLD PLATED COPPER WIRE	1. 99.99% COPPER 2. GOLD PLATED	1. Tolerance - THICKNESS: $\pm 0.01$ - WIDTH: $\pm 0.04 - 0.02$ 2. ELONGATION(%): 10 MORE THAN 3. TENSION: (KGF) 0.2 MORE THAN 4. GOLD THICKNESS: $0.05 \mu\text{m MIN}$ *MAKER: TAIHAN ELECTRIC plating process: JMBCEON/SUNSEUN
2. INSULATION	POLYESTER FILM (PET/PET)	1. POLYESTER BASE FILM : $0.025 \text{ mm}$ 2. POLYESTER HOTMELT ADHESIVE : $0.035 \text{ mm}$ TOTAL : $0.060 \text{ mm}$ THICKNESS	UL VW-1 FLAME Width : $120 \text{ mm}$ Length : $500 \text{ M}$ UNIT : ROLL *MAKER: SHINCHANG HOTMELT/ COSMOAMT
3. SUPPORTING TAPE	POLYESTER FILM	1. POLYESTER BASE FILM : $0.188 \text{ mm}$ 2. POLYESTER HOTMELT ADHESIVE : $0.027 \text{ mm}$ TOTAL THICKNESS : $0.215 \text{ mm}$ TOTAL THICKNESS : $0.065 \text{ mm}$	Width : $20.5 \text{ mm}$ Length : $250 \text{ M}$ Unit : ROLL *MAKER: SUNGSHIN Trading/ COSMOAMT
4. SILICON TAPE (BROWN)			*MAKER: DAEHYUN ST

## ◆ Note

- Pad : GOLD Plating
- $\# \geq \text{Cpk } 1.0$
- $\#\# \geq \text{Cpk } 1.33$
- Stiffener color : Sky Blue
- H-F
- Dimensions unit : mm



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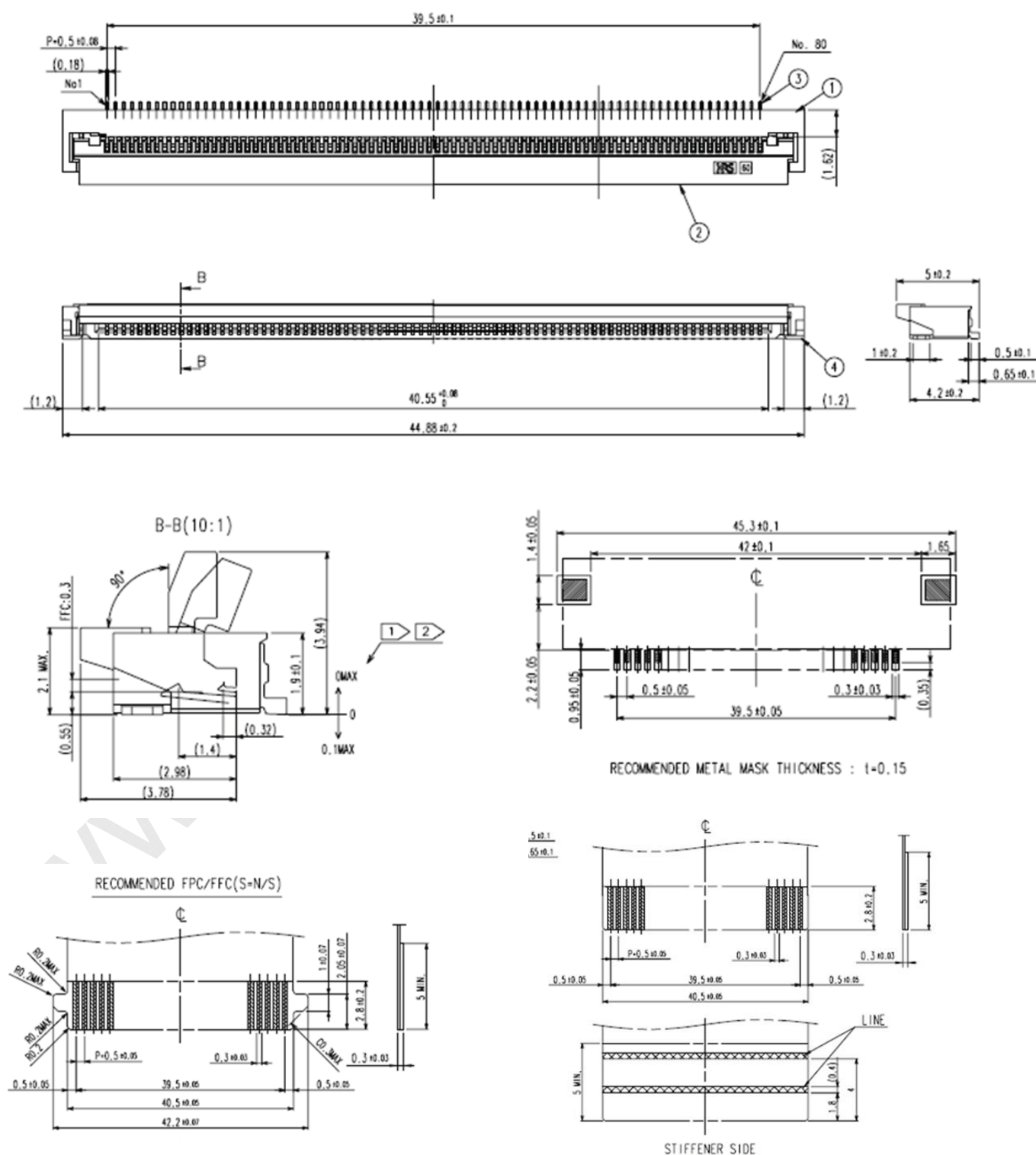
## Product Specification

## # APPENDIX-VIII

## ■ FFC CONNECTOR INFORMATION

- LCD Connector : TF06L-80S-0.5SH (Manufactured by HRS) or Compatible

## ■ Drawing (TF06L-80S-0.5SH\_Manufactured by HRS)



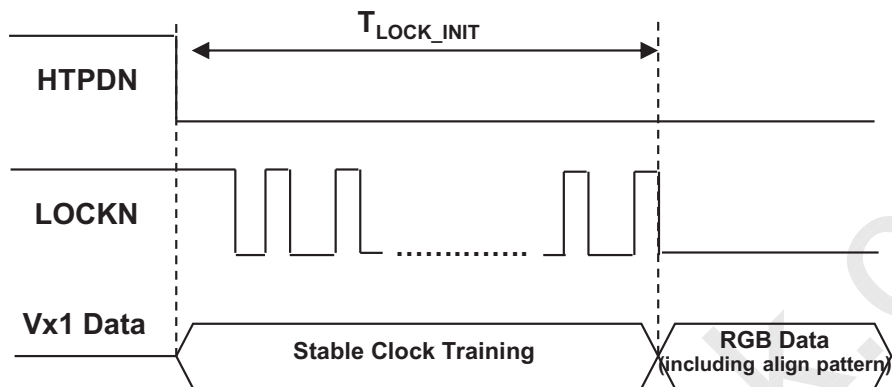
Ver. 1.2

LC860EQY

## Product Specification

## # APPENDIX-VIII-1

## ■ Vx1 Initialization Characteristics



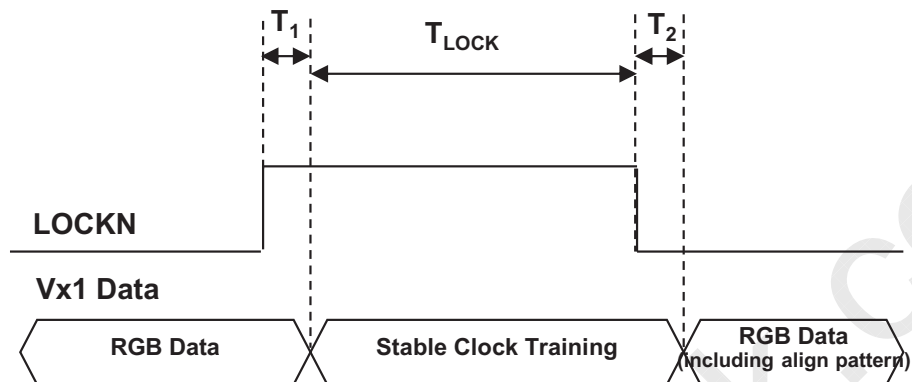
## \* UHD60Hz T-Con

Characteristics	Symbol	Min	Typ	Max	Unit
Initial CDR lock time (From Stable CDR training to CDR lock)	$T_{LOCK\_INT}$	0		310	ms

## Product Specification

## # APPENDIX-VIII-2

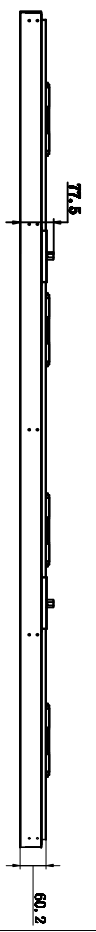
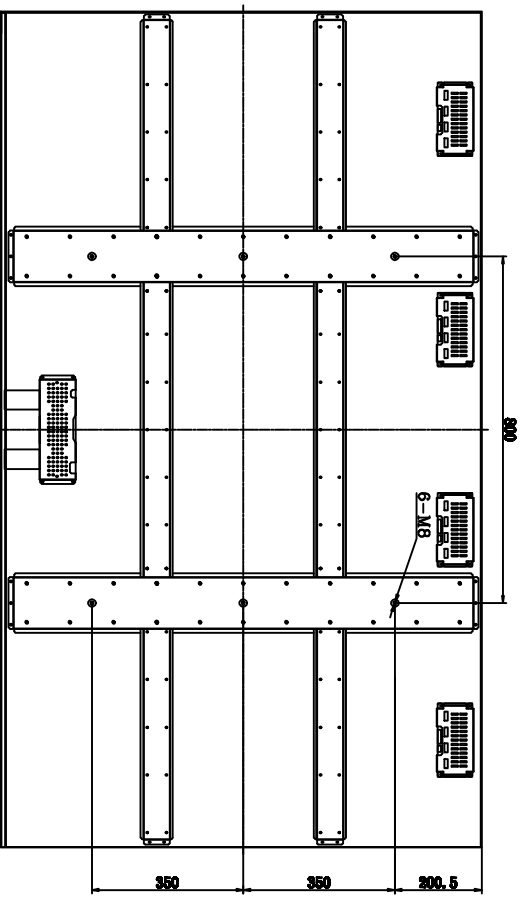
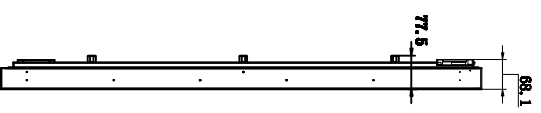
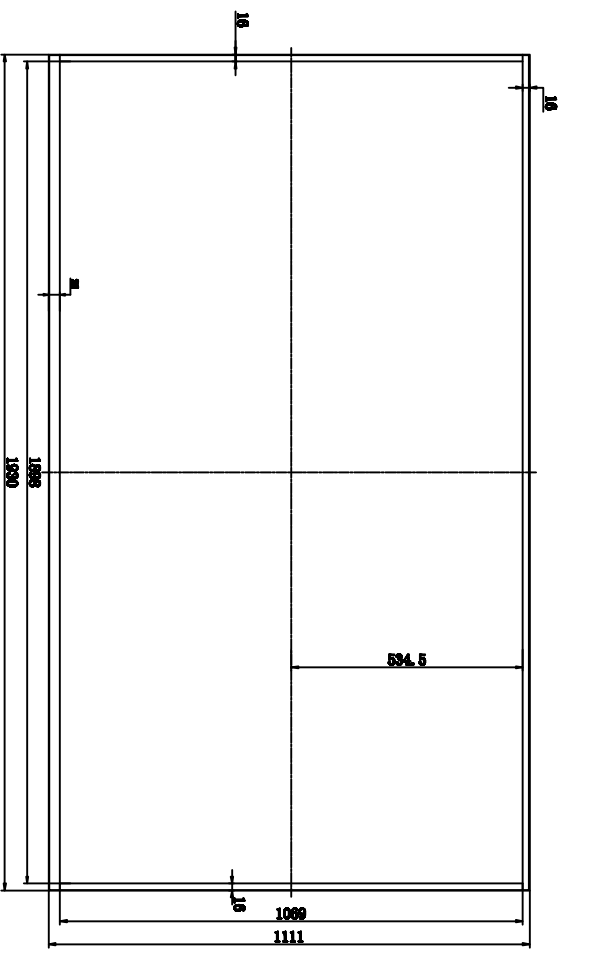
## ■ Vx1 Lock Timing In Normal Operation



Characteristics	Symbol	Min	Typ	Max	Unit
CDR lock time from stable clock training pattern to LOCKN “Low” in normal operation	$T_{LOCK}$			2	ms
Latency from LOCKN “High” to clock training pattern	$T_1$			100	us
Latency from clock “Low” to normal RGB Data	$T_2$			100	us

※ Vx1 Rx should get clock training pattern in  $T_1$

※ Vx1 Rx should get RGB Data (including align pattern) in  $T_2$



880085-GEZT-01  
规格书